STRUCTURAL AND ELECTRICAL PROPERTIES OF EPITAXIAL GRAPHENE NANORIBBONS

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DEDICATION

To Francisco, my love, my friend, my constant sounding board, and my biggest fan.

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LIST OF ABBREVIATIONS AND SYMBOLS

CMOS	Complementary-metal-oxide-semiconductor
FET	Field-effect transistor
MOSFET	Metal-oxide-semiconductor field-effect transistor
ITRS	International Technology Roadmap for Semiconductors
IEN	Institute for Electronics & Nanotechnology
1D	One-dimensional
2D	Two-dimensional
ExG	Exfoliated graphene
EG	Epitaxial graphene
GNRs	Graphene nanoribbons
LER	Line edge roughness
QFS-MG	Quasi-free-standing monolayer graphene
QFS-BG	Quasi-free-standing bilayer graphene
SiC (0001)	Si-face of SiC substrates
SiC $(000\bar{1})$	C-face of SiC substrates
HI	Hydrogen-intercalated
HI-GNR	Hydrogen-intercalated GNR
AG	As-grown
AG-GNR	As-grown GNR
CVD	Chemical vapor deposition
SEM	Scanning electron microscope
XPS	X-ray photoelectron spectroscopy
AFM	Atomic force microscope
UHV	Ultrahigh vacuum
UV	Ultraviolet
EBL	Electron-beam lithography
e-beam	Electron-beam
DI	Deionized
RIE	Reactive Ion Etcher
ALD	Atomic-layer deposition
RF	Radio-frequency
CMP	Chemical-mechanical polishing
H or H_2	Atomic or molecular hydrogen
Si	Silicon
C	Carbon
O	Oxygen
Ar	Argon
Cu	Copper
Ti	Titanium
Au	Gold
SiC	Silicon carbide
SiO_2/Si	Oxidized silicon substrates

HSQ	Hydrogen silsesquioxane
HF	Hydrofluoric acid
Å	Angstrom
nm	Nanometer
µm	Micrometer/micron
mm	Millimeter
cm	Centimeter
m	Meter
GHz	Gigahertz
V	Volts
eV	Electron-volts
A	Amperes
µA	Micro-amperes
nA	Nano-amperes
W	Watt
s	seconds
min	minutes
K	Kelvin
°C	Degrees Celsius
sccm	Standard cubic centimeters per minute
I	Current
V or V_G or V_H	Voltage or gate voltage or Hall voltage
R	Resistance
R_S	Sheet resistance
E	Energy
E_F	Fermi energy
E_{gap}	Energy gap
$sgn( )$	Sign (negative/positive) of value in ( )
P	Pressure
T	Temperature
t	Time
I_{on}/I_{off}	On-off current ratio
n	Charge carrier density
q	Electronic charge
σ	Conductivity or pseudospin
μ	Charge carrier mobility
μ_{GNR}	GNR mobility
μ_{2D}	Two-dimensional mobility
μ_W	LER-limited mobility
ρ	Resistivity
V_{Gmin}	Minimum conductivity point, charge-neutrality point, Dirac point
v_F	Fermi velocity
$\hbar$	Planck's constant divided by 2π
k	Momentum
W	GNR line width
L	GNR length

W_T	Terrace width
W_{th}	Threshold line width
Ω or Ω/□	Ohms or Ohms per square (sheet resistance)
B	Magnetic field strength
F	Farads
$\mu C/cm^2$	Micro-Coulombs per unit area
C_G	Gate capacitance

SUMMARY

The objective of this research was to perform a systematic investigation of the unique structural and electrical properties of epitaxial graphene at the nanoscale. As the semiconductor industry faces increasing challenges in the production of integrated circuits, due to process complexity and scaling limitations, new materials research has come to the forefront of both science and engineering disciplines. Graphene, an atomically-thin sheet of carbon, was examined as a material which may replace or become integrated with silicon nanoelectronics. Specifically, this research was focused on epitaxial graphene produced on silicon carbide. This material system, as opposed to other types of graphene, holds great promise for large-scale manufacturing, and is therefore of wide interest to the academic and industrial community.

In this work, high-quality epitaxial graphene production was optimized, followed by the process development necessary to fabricate epitaxial graphene nanoribbon transistors for electrical characterization. The structural and electrical transport properties of the nanoribbons were elucidated through a series of distinct experiments. First, the size-dependent conductivity of epitaxial graphene at the nanoscale was investigated. Next, the alleviation of the detrimental effects revealed during the size-dependent conductivity study was achieved through the selective functionalization of graphene with hydrogen. Finally, two techniques were developed to allow for the complementary doping of epitaxial graphene. All of the experiments presented herein reveal new and important aspects of epitaxial graphene at the nanoscale that must be considered if the material is to be adopted for use by the semiconductor industry.

CHAPTER I – INTRODUCTION

1.1 HISTORY OF THE PROBLEM

Since the inception of the semiconductor industry in the middle of the twentieth century, the evolution of integrated circuits has been largely governed by Moore's Law, which states that the number of transistors on a single chip doubles approximately every two years. Originally postulated in 1965 [1] by Gordon E. Moore, co-founder of Intel Corporation, Moore's Law suggests that the exponential trend in silicon (Si) device scaling will hit a fundamental roadblock when transistor dimensions begin to approach the atomic scale. In a traditional metal-oxide-semiconductor field-effect transistor (MOSFET), the building block of most integrated circuitry, there are two key components that influence the behavior of the device: the physical distance between the source and the drain (i.e., the channel length or technology node) and the gate insulator thickness. The continued shrinking of both these dimensions, as required by Moore's Law, has led to ever-increasing problems with power consumption, as shorter channel length and reduced gate insulator thickness lead to excessive leakage current and increased power consumption.

In the past year, Intel Corporation has attempted to circumvent the problems associated with silicon device scaling by creating the first three-dimensional field-effect transistor (FET) structure for the 22-nanometer (nm) generation. The new device architecture, known as a tri-gate transistor or FinFET, is predicted to remain successful in terms of performance and production cost down to the 10-nm node [2]; beyond that, further innovations will be required. One of the key issues plaguing further use of the

FinFET architecture below the 10-nm node is the stringent process conditions necessary to fabricate devices at the nanoscale. Specifically, for the 20-nm node FinFET, the dimensions of the fin itself must be controlled to within a 0.5-nm accuracy [3]; this level of precision must also be maintained throughout every subsequent processing step. Such strict fabrication requirements lead to large variation in devices across a conventional 300 millimeter (mm) silicon wafer, which in turn affects the yield over a range of technology nodes [4]. Furthermore, uniform doping of such a small structure is extremely challenging, and the nonuniformity of dopants can lead to significant power loss. These issues, which continue to plague the further scaling of silicon devices, are forcing the semiconductor industry to consider alternate solutions. Beyond utilizing novel device architectures such as the FinFET, the International Technology Roadmap for Semiconductors (ITRS) states that a likely solution to the scaling challenge will be based on nonclassical materials for integrated circuit production beyond 2017 [2]. Various material systems have been considered for integration with current silicon technology, including semiconducting nanowires, III-V materials, thin metal films, germanium, carbon (C) nanotubes, and most notably, graphene.

Graphene, a two-dimensional (2D) hexagonal array of carbon atoms, has become a material of intense interest to both the scientific and industrial communities in the past decade. The inherently small dimensionality and exceptional electronic, thermal, and mechanical properties of graphene make this material one of the prime candidates for future integrated circuit production. Graphene can be produced through a variety of methods including mechanical exfoliation of highly-oriented pyrolitic graphite onto oxidized silicon (SiO_2/Si) substrates [5], chemical vapor deposition (CVD) on metallic

thin films [6, 7], chemical reduction of graphene oxide [8], and by the sublimation of silicon atoms from single-crystal silicon carbide (SiC) [9]. Exfoliated graphene (ExG) is the most common and least expensive method of graphene production, but the painstaking flaking process and subsequent manual identification of monolayer and bilayer graphene regions makes this method ill suited for mass production. Both CVD growth and graphene oxide reduction require that the graphene be transferred to alternate substrates, usually SiO_2/Si, which also limits the quality of the material and the throughput of such methods. In contrast, the sublimation method from SiC, which produces epitaxial graphene (EG), represents a legitimate route to large-scale manufacturing. The synthesis of EG layers across a large-area SiC wafer allows for a truly monolithic system to be envisioned, where the transistor and interconnect material can be seamlessly integrated. Silicon carbide has long been used in power electronics as a result of the ability of the material to operate at high temperatures and voltages, but the discovery in 1974 of graphitic films forming on the substrate surface when heated to high temperature [10] has recently led to a significant push in the scientific community to perfect the synthesis of EG on SiC substrates.

As a result of the ease with which ExG can be produced, most research focusing on the electronic behavior of graphene devices has been confined to this particular material. In comparison, there is a distinct deficit of information pertaining to the unique structural and electronic properties of EG devices fabricated on SiC substrates, especially in the context of nanoribbons, which are defined as structures with a line width less than one micron (μm). In terms of digital logic devices, the interest in graphene nanoribbons (GNRs) stems from the intrinsic lack of a semiconducting band gap in the material.

Without a band gap, graphene logic devices are not fully realizable due to the severely limited switching ability and the relatively large off-state conductivity. A number of methods have been studied that can effectively induce a band gap in graphene, including the application of a perpendicular electric field to bilayer graphene [11] and the functionalization of graphene with atomic hydrogen [12]. In addition, the quantum confinement of charge carriers in narrow graphene regions (i.e., GNRs) has been shown to induce a band gap [13] that may allow for improved switching behavior in logic devices. Transport or mobility energy gaps, attributed to edge disorder in GNRs, have also been achieved [14], furthering the desire to understand and exploit this unique property of GNRs. Outside the realm of logic devices, GNRs can also be successfully used for analog or radio-frequency (RF) FETs. Most notably, IBM researchers demonstrated a 100 gigahertz (GHz) graphene transistor fabricated from wafer-scale EG on SiC substrates with a gate length of 240 nm [15]. An identically-sized silicon FET can only achieve a cut-off frequency of ~ 40 GHz, which clearly demonstrates the impressive performance afforded by graphene electronic devices. Additionally, GNRs are also an important topic of study in the context of electrical interconnects. When considering the prevalent interconnect material in integrated circuits, copper (Cu), the resistivity is found to rise sharply as the line widths are successively scaled down as a result of grain boundary and sidewall scattering [2]. Graphene, especially wafer-scale EG, can be used simultaneously as the channel material for devices and for interconnects, therefore graphene has become a candidate material to replace Cu as interconnect dimensions continue to shrink. The myriad uses of GNRs – band gap induction, RF FETs,

interconnects – lead to a pressing need to fully understand the unique phenomena and performance limitations encountered when making use of these structures.

Although very similar, exfoliated and epitaxial graphene exhibit some strikingly disparate behaviors, many of which are a direct result of the different substrate support systems. The ability to produce continuous films of EG at the wafer scale, something impossible at this point for ExG, leads to the necessity to fully investigate and understand the unique behavior of the material system. Furthermore, the unique properties associated with GNRs necessitate a systematic investigation of the interplay between structural and electronic properties of EG at the nanoscale. For this reason, the research in this work was mostly confined to the production of EG and the investigation of the novel properties of epitaxial GNRs in the context of logic devices.

1.2 GRAPHENE FUNDAMENTALS

The term "graphene" was first defined in 1994 as "the individual carbon layers in graphite intercalation compounds" [16]. Long before the nomenclature was made official, graphene had been studied theoretically in band structure calculations as a single layer of graphite [17, 18]. Experimentally, the only evidence of thin graphitic layers was found on the surface of SiC after the substrate was heated in vacuum [10]. Although graphite is technically composed of individual monolayers of hexagonally-arranged carbon atoms, or graphene, the isolation of such a 2D crystal was widely believed to be thermodynamically unstable [19, 20] and therefore impossible to isolate in an experimental setting. This idea was disproved in 2004 when researchers at the University of Manchester became the first to successfully isolate monolayers of graphite through a mechanical exfoliation method

[5]; adhesive tape was used to remove individual layers from highly-oriented pyrolytic graphite and the resulting material was transferred to an SiO_2/Si substrate. Monolayer and few-layer graphene were identified through a combination of optical and atomic force microscope (AFM) imaging. Few-layer graphene was patterned into a Hall bar structure to study the electronic properties of the material, and a metallic field-effect transistor was realized. This seminal work later earned Andre Geim and Konstantin Novoselov, the leaders of the University of Manchester group, the 2010 Nobel Prize in Physics, and is heralded as the starting point for an intense period of research into graphene electronics. Less than a year after their initial discovery, Geim and Novoselov successfully performed the first electronic transport measurements on monolayer graphene [21], and reported behavior similar to that witnessed for few-layer graphene.

Bulk graphite is made up of a periodic arrangement of individual graphene layers held together by van der Waals forces with an interlayer spacing of 3.4 Angstroms (Å). Individual graphene monolayers are composed of a hexagonal array of carbon atoms spaced 1.42 Å apart and held together by the strong C-C σ-bond between three of the four valence electrons (Figure 1.1).

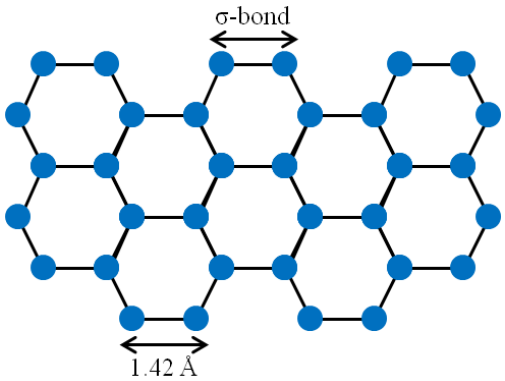

Figure 1.1. The hexagonal lattice of graphene.

These bonds allow graphene to exhibit a high level of mechanical strength, even though the material is atomically thin. The fourth valence electron is found perpendicular to the graphene layer in the molecular p-orbital and participates in electronic conduction. Collectively, neighboring electrons in the p-orbital of individual C atoms form π-bands, and conduction occurs within these bands [22].

In 1947, Phillip Wallace described the electronic structure of graphite using the tight-binding approximation [17], and revealed a unique band structure that makes a single atomic layer of graphite (i.e., graphene) exceedingly different from most materials. In a traditional semiconductor, the energy bands that represent the forbidden electronic states of charge carriers in the material are split into two parabolic regions, the valence band and the conduction band. The band gap is defined as the energy difference between the upper region of the valence band and the lower region of the conduction band. In contrast, the band structure of graphite is conical in shape at low energies near the corners of the Brillouin zone, the fundamental cell in momentum space (Figure 1.2).

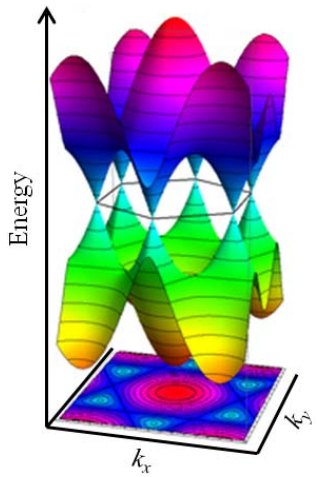

Figure 1.2. The band structure of graphene.

The valence and conduction bands at these points intersect, thereby classifying graphene as a gapless semimetal. The conical energy dispersion in momentum space is mathematically expressed as

$$E = \hbar v_F \sqrt{{k_x}^2 + {k_y}^2}\,, \tag{1.1}$$

where $\hbar$ is Planck's constant divided by 2π, k_x and k_y represent the momentum vectors in two dimensions, and v_F describes the Fermi velocity. Unique to graphene and one of the root causes for the high charge carrier mobility of the material is the value of the Fermi velocity, $v_F \sim 1 \times 10^6$ m/s, which is constant for charge carriers in graphene [23].

The linear energy dispersion quickly gives rise to an analogy with photons, massless elementary particles that travel with constant velocity and also exhibit a linear energy dispersion relationship. This relationship leads to a stark difference in the way that charge carriers in graphene behave as compared to conventional metals and semiconductors; as a result, charge carriers in graphene are often referred to as quasiparticles. At positive energies, these quasiparticles behave as normal electron-like states with negative charge; at negative energies, the unoccupied electronic states behave as hole-like positively-charged quasiparticles. Typically for such a system, the behavior of the charge carriers would be described by two distinct wavefunctions that are not connected in any way. However, the unusual symmetry of the graphene lattice adds another requirement that forces the electron-like and hole-like quasiparticle states in graphene to be interconnected. The fundamental unit cell of graphene contains two equivalent atoms that, when the lattice is viewed as a whole, form two independent, crystalline Sublattices A and B (Figure 1.3).

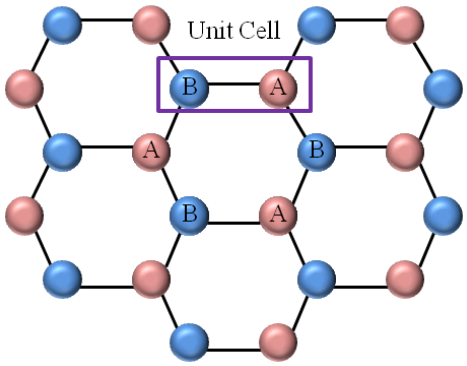

Figure 1.3. The A and B sublattices of graphene.

This type of lattice arrangement requires the consideration of an extra degree of symmetry that is analogous to charge conjugation symmetry in quantum electrodynamics, the branch of physics that describes the interaction of light and matter by taking into account relativistic quantum mechanics. The symmetry requirement calls for the use of a two-component wavefunction to accurately characterize the system, one component to describe the contribution from each sublattice. Such a two-component wavefunction is analogous to the description of spin systems, namely the behavior of fermions that constitute all fundamental particles of half-integer spin, such as electrons. Therefore, in graphene, the term pseudospin is used to differentiate between the contributions from the individual Sublattices A and B, and is analogous to the individual contributions (i.e., spin up and spin down) in the Dirac equation for fermions. These analogies allow the total energy of the system near the corners of the Brillouin zone to be characterized using a Dirac-like Hamiltonian [24] of the form:

$$H = \hbar v_F \boldsymbol{\sigma} \cdot \boldsymbol{k} \,, \tag{1.2}$$

where $\boldsymbol{\sigma}$ represents the Pauli spin matrices (i.e., pseudospin contributions) and $\boldsymbol{k}$ represents the momentum vector. This equation describes the behavior of the relativistic,

massless, fermion-like quasiparticles that exist in graphene. For this reason, the charge carriers in graphene are commonly referred to as Dirac fermions. Similarly, the region of linear energy dispersion is referred to as the Dirac cone, and the intersection of the conduction and valence bands is known as the Dirac point (V_{Dirac}) (Figure 1.4).

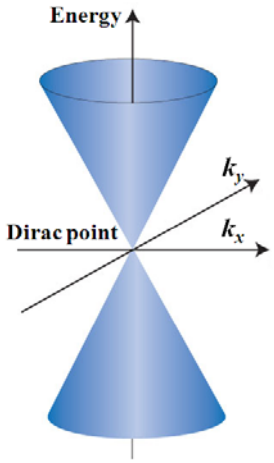

Figure 1.4. The linear energy dispersion of graphene at the corners of the Brillouin zone.

The unusual symmetry found in the graphene lattice and the subsequent necessity to consider pseudospin is another contribution to the superior conductivity of graphene. Charge carriers effectively hop between sublattices during conduction, and as a result, these sublattices serve as a type of degree of freedom that is described by the pseudospin (σ). The fact that the two sublattices must exhibit opposite pseudospin to be accurately described by Equation 1.2 leads to a unique and amazing property of graphene, as described pictorially in Figure 1.5.

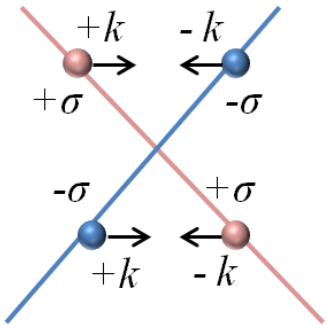

Figure 1.5. The pictorial representation of pseudospin in graphene. Light pink signifies energy dispersion and quasiparticles belonging to Sublattice A, and light blue signifies energy dispersion and quasiparticles belonging to Sublattice B. Pseudospin (σ) and momentum (k) vectors are shown for electrons (upper cone) and holes (lower cone).

An electron traveling in the positive direction with energy E in the conduction band and a hole traveling in the negative direction with energy $-E$ in the valence band are found to belong to the same branch of the energy dispersion for a particular sublattice (i.e., A). Both the electron and hole in Sublattice A have the same pseudospin, where the pseudospin is parallel to momentum for electrons and antiparallel to momentum for holes. When considering an electron in the conduction band belonging to the other sublattice (i.e., B), the pseudospin and momentum are opposite to that of the electron in Sublattice A; the same is true for the holes in the valence band of Sublattice B. The consequence of this orientation is that backscattering within either the conduction or valence band is forbidden. For backscattering to occur, the sign of the momentum must be switched, which would also require an identical switch in the sign of the pseudospin. Any change in the sign of the pseudospin is generally disallowed, and can only be accomplished via short-range perturbations that would act differently on the A and B sublattices [25]. Long-range perturbations, such as those created by the influence of surrounding materials, would affect both sublattices uniformly, and the sign of the

pseudospin could not be switched in that case. Without the influence of backscattering, graphene can exhibit ballistic transport at room temperature, where charge carries can travel up to μm-scale distances before experiencing a scattering event [26]. The unique behavior of Dirac fermions in graphene as a result of pseudospin, and the subsequent lack of backscattering, is another reason for the extremely high conductivity of the material.

Although graphene is known to exhibit a number of interesting physical and electrical phenomena, such as electron focusing by a Veselago lens [27] and angle-dependent Klein tunneling [25], this work focuses on the superior conductivity of graphene and the implications of this aspect of the material. In comparison to silicon [28], which displays a room temperature charge carrier mobility (μ) for electrons of $\mu \sim 1400$ $cm^2/V\text{-}s$ at the intrinsic charge carrier density (n) of $n \sim 10^{10}$ cm^{-2}, graphene produced by all of the methods described above exhibits significantly larger mobilities. Table 1 outlines these values for exfoliated, CVD, and epitaxial graphene. Although fabrication and processing can lower the theoretically-predicted mobility and charge carrier density values for graphene of various types, the mobility is still expected to outperform what is currently afforded by conventional silicon devices.

Table 1. Room temperature silicon vs. graphene mobility.

	Silicon	**Exfoliated Graphene**	**CVD Graphene**	**Epitaxial Graphene**
Mobility ($cm^2/V\text{-}s$)	1400	**SiO_2/Si:** 4×10^4 **Suspended:** 1.2×10^5	4000	**Si-face:** 3×10^4 **C-face:** 2.5×10^5
Charge carrier density (cm^{-2})	10^{10}	10^{10}	10^{11}	10^{10}

1.3 EPITAXIAL GRAPHENE NANORIBBONS

The intrinsic zero-gap semimetal nature of graphene makes the material a less than desirable candidate for digital logic devices, as the ability to switch the device is severely limited. Initial experiments of gated graphene on various substrates showed extremely modest on-off current ratios (I_{on}/I_{off} = 5-30), which are nowhere near what is currently required in traditional silicon MOSFETs. The ITRS states that any alternative material used in future logic devices is expected to exhibit on-off current ratios between 10^4 and 10^7 [2]. As a result of many of the exceptional properties of graphene, including the mobility, thermal conductivity, and mechanical strength, a majority of research has been devoted to improving the switching capabilities of graphene in the hope of making the material a viable candidate for post-silicon logic.

As a result of the necessity to keep device dimensions at the nanoscale as required by the scaling trend of silicon, the use of nanoribbons as a way to induce a band gap is widely considered to be the most elegant and useful methodology. When graphene is changed from a 2D material to a one-dimensional (1D) system via lateral confinement (i.e., nanoribbon formation), the 2D energy dispersion is expected to split up into multiple 1D modes. Some of these modes may not pass through the Dirac point, and thus could exhibit a finite energy gap [29]. In essence, charge carriers moving through the nanoribbon would be laterally confined with changes in electrical transport being governed by the structure of the nanoribbon edge. Pristine GNRs are expected to display either an armchair or a zigzag edge, and, therefore, most theoretical calculations of energy gap induction are based on these two orientations (Figure 1.6).

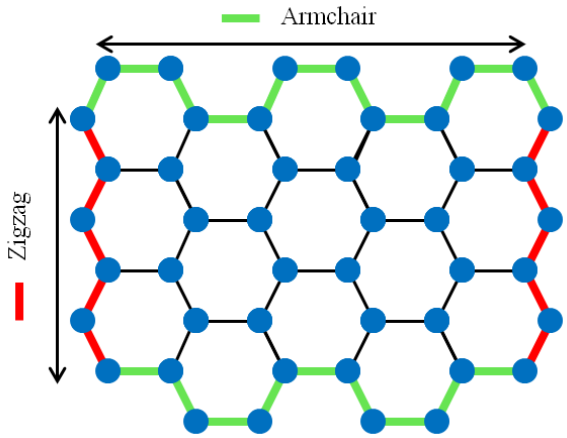

Figure 1.6. The pristine armchair and zigzag edges of a graphene nanoribbon.

Theoretically, the size of the induced energy gap is a direct function of the nanoribbon width [30, 31], as expressed by

$$E_{Gap} = \frac{\alpha}{W}, \tag{1.3}$$

where the parameter $\alpha \sim 0.2\text{-}1.5$ eV/nm, W is the width of the nanoribbon in nm, and E_{gap} is the size of the induced energy gap measured in electron-volts (eV). The major issue regarding this theoretical estimation is the presence of nonidealities encountered during GNR fabrication. The most widely used fabrication method is based on the exposure of negative-tone resist with an electron-beam (e-beam) lithography system and subsequent plasma etching to remove the excess graphene not protected by the etch mask. The result of such an exposure is a roughened edge that is not atomically smooth, and thus is neither armchair nor zigzag. Recent studies of chemically-derived GNRs formed from the unzipping of carbon nanotubes have shown a reduction in the line-edge roughness (LER) induced by e-beam lithography, but the GNR edges were still not found to be purely zigzag or armchair [32].

In 2007, the first electrical measurements of energy gap induction in exfoliated GNRs were performed [33]. Due to the lithographically-patterned LER, the energy gap expression was modified to

$$E_{Gap} = \frac{\alpha}{(W - W_0)}, \tag{1.4}$$

where the parameter W_0 signifies the size of the inactive channel region. Localized edge states can render regions of the nanoribbon inactive in conduction; therefore, the use of the full width of the nanoribbon (W) alone does not provide the best estimate of the induced energy gap. In addition, under-cutting of the etch mask during plasma processing can result in a reduced width of the conducting region. In contrast to the theoretical calculations based on ideal GNR edges, the calculated size of the energy gap based on experiment was found to be significantly larger than predicted.

The unexpected results have led to a number of theories being put forward to explain the discrepancy in the size of the energy gap. One popular theory is based on the formation of a Coulomb blockade as a direct result of the roughened GNR edges [34]. Line-edge roughness leads to localized states at the GNR edge, which results in a nonuniform ribbon width. In certain regions of the GNR, the conducting channel is significantly narrower than desired, which causes a large decrease in conduction in these regions. The result over the length of the GNR is a series of dots, akin to quantum dots, in which charges can easily become trapped. This type of structure leads to the formation of a Coulomb blockade, through which electrons are able to tunnel with the application of an external bias. The second theory, Anderson localization, also incorporates the effect of edge disorder in GNRs. In essence, in the presence of multiple, short-range scattering sites, such as those provided by the rough GNR edges, the electrons become localized in

a finite region and cannot travel over long distances [35]. Both of these theories manifest in experiment as the induction of a transport gap, which is not identical to or caused by the same physical phenomena that create a true band gap within 1D graphene regions.

After the proposal of such theories and the discovery of a discrepancy in the size of the energy gap determined from theory and experiment, Han *et. al* reproduced their initial experimental work and performed additional analysis [14]. The results of that work suggest that edge disorder in GNRs lead to the induction of a transport gap, not a band gap, which both behave similarly in an electronic sense, but are not caused by the same fundamental physics. For exfoliated GNRs on SiO_2/Si substrates, the transport gap is found to be as large as 0.3 eV for a GNR width of ~ 15 nm, and negligible gaps (< 0.01 eV) are even observed for GNR widths up to 90 nm [33]. In comparison to silicon, which exhibits a band gap of 1.1 eV, this value may seem trivial, but GNRs with widths less than 15 nm are expected to exhibit significantly larger transport gaps.

As of yet, only limited data has been provided to support the conclusion that similarly-sized band gaps or transport gaps can be induced in epitaxial GNRs. This is a result of the combined effect of the lack of EG research and the limited availability of e-beam lithography tools capable of producing feature sizes less than 20 nm. Epitaxial GNRs on *6H*-SiC substrates fabricated with the e-beam resist hydrogen silsesquioxane (HSQ) exhibit a band gap of ~ 0.15 eV for a GNR width of ~ 10 nm [36]. The switching capability is found to lie in the expected range at room temperature (I_{on}/I_{off} ~ 10), but this value rises substantially to 10^6 at a temperature of four Kelvin (K). Such results suggest that sub-10-nm epitaxial GNRs may be capable of providing improved switching performance even at room temperature. In addition, epitaxial GNRs fabricated with a

novel technique, whereby patterned SiC substrates are used to selectively graphitize narrow regions without the need for etching or lithography, also show preliminary proof that band gap induction is possible for GNRs as wide as 250 nm at a temperature of 4 K [37]. Both of these results necessitate further research into the use of epitaxial GNRs as logic devices, specifically by investigating the limitations encountered by such devices.

1.4 OVERVIEW OF THE RESEARCH

The research presented herein is broken up into four distinct tasks aimed at elucidating the unique structural and electrical properties of epitaxial GNRs, investigating the electrical behavior of such devices in the context of transistor operation, and providing improvements to the technology. The first task undertaken, presented in Chapter II, is the optimization of process conditions to produce high-quality EG on SiC substrates. The development of both the hydrogen-etching process of as-received SiC to remove the chemical-mechanical polishing (CMP) damage, and the subsequent graphitization process to synthesize monolayer graphene is reported. To quantify the results of the hydrogen etching and graphitization processes, the structural and electrical characterization procedures used to confirm the growth of high-quality EG on the Si-face of SiC substrates are presented. The second task, presented in Chapter III, is two-fold: to develop the process flow necessary to create electrical devices capable of probing the conductivity of epitaxial GNRs, and to provide a careful study of the conductivity of epitaxial GNRs fabricated in the nanoscale regime (10 nm < W < 1 μm). Specifically, the size-dependent conductivity of epitaxial GNRs is reported; a strong correlation between the charge carrier mobility and both the lithographically-patterned LER and the substrate

morphology is suggested. The third task, presented in Chapter IV, is focused on the selective hydrogenation of GNR edges; this process has been predicted to reduce the influence of LER scattering and provide a route to improving the size-dependent conductivity in nanoscale graphene. The fourth task, presented in Chapter V, tackles the issue of removing or counteracting the intrinsic, strong, n-type doping of epitaxial GNRs on the Si-face of SiC substrates; this level of n-type doping makes complementary doping of the graphene problematic. This task is also two-fold: first, thermal annealing of the e-beam resist HSQ is used to counteract the n-type doping, and then a hydrogen intercalation process is developed which can similarly remove the n-type doping and allow for p-type graphene to be realized. All of the research presented herein focuses on obtaining a clear picture of EG behavior at the nanoscale, and improving the issues which plague the use of epitaxial GNRs in future nanoelectronics.

CHAPTER II – EPITAXIAL GRAPHENE GROWTH AND CHARACTERIZATION

The objective of the first part of the research was to obtain and characterize high-quality EG on SiC substrates in line with what has previously been presented in the literature. The major goals of this objective were:

1) to remove the CMP damage from the as-received SiC substrates, and thereby achieve atomically-smooth, stepped surfaces via the hydrogen-etching procedure;
2) to optimize the graphitization process for both the polar faces (the Si-face and the C-face) of the SiC substrates;
3) and to characterize the structural and electrical properties of the as-grown (AG) graphene on both the polar faces of the SiC substrates.

The successful completion of these objectives was the foundation of all subsequent research, as the optimized hydrogen-etching and graphitization procedures are shown to be capable of producing high-quality EG. The produced EG was used in the remainder of this work to investigate the structural and electrical properties of EG at the nanoscale.

2.1 EPITAXIAL GRAPHENE ON SILICON CARBIDE SUBSTRATES

As mentioned previously, graphitic thin films were found to "grow" on the surface of SiC substrates [10] as long ago as 1974, but the idea of intentionally graphitizing the SiC surface for use in electronic devices was not considered until 2004 [9]. The de Heer group at the Georgia Institute of Technology provided the initial

electronic transport measurements of EG in the same year as the seminal ExG experiments by the University of Manchester group. For multilayer ExG on SiO_2/Si substrates, the room temperature graphene mobility was found [5] to range between μ = 3000-10,000 cm^2/V-s at a charge carrier density of $n \sim 10^{12}$ cm^{-2}. The FET used exhibited an on-off current ratio of $I_{on}/I_{off} \sim 30$. In comparison, for monolayer graphene on the C-face of SiC substrates [9], the room temperature mobility was measured to be μ = 2.7 x 10^5 cm^2/V-s at a charge carrier density of $n \sim 10^{16}$ cm^{-2}. Later work based on similar EG material patterned into FET structures demonstrated $I_{on}/I_{off} \sim 5$ for Si-face graphene [38]. Although the switching ability of the early EG FET experiments was significantly less than that found for ExG, the large mobility values obtained for the epitaxial samples led to an explosion of interest in the field of EG research.

The majority of the SiC substrates used for EG growth are hexagonal polytypes *4H* or *6H*, where the numeral refers to the number of SiC bilayers within the unit cell of each polytype. To be useful for electrical measurements, the SiC must be semi-insulating, which is easily obtained with *4H* polytypes. Most *6H* polytypes are manufactured with dopants, so that the substrate is conductive and, therefore, not useful to measure the electrical properties of the graphene film grown on the surface. Upon comparing the charge carrier density and the mobility of the EG grown on both semi-insulating *4H*- and *6H*-SiC substrates [39], no distinct differences were found between the graphene produced on the two polytypes. In this research, semi-insulating *4H*-SiC substrates were used to produce EG due to the accessibility of the material.

The *4H*-SiC substrates have a hexagonal crystal structure, one of the reasons for the high level of epitaxy with graphene, composed of bilayers of planar sheets of Si and

C atoms spaced 0.25 nm apart; the unit cell is composed of four such bilayers. Silicon carbide contains two species-terminated faces: the silicon-terminated face, SiC (0001) or the Si-face, and the carbon-terminated face, SiC $(000\bar{1})$ or the C-face (Figure 2.1).

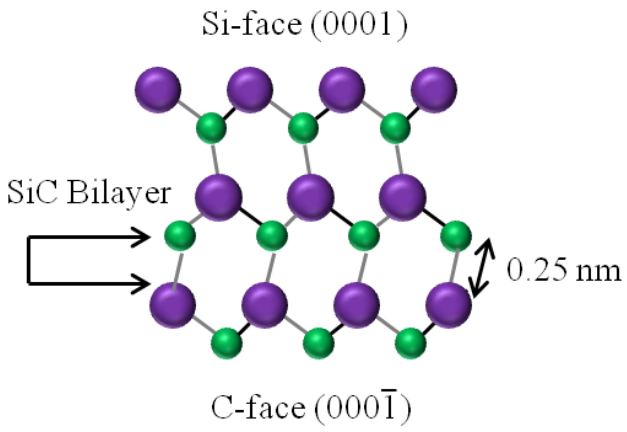

Figure 2.1. The atomic structure of *4H*-SiC with two polar faces. Silicon atoms are shown in purple, carbon atoms in green.

The growth mechanism on each polar face is distinctly different, as is the electrical behavior of the produced EG. Growth on the Si-face proceeds slowly and is self limiting, so that no more than a few layers of EG can be produced [40]. In contrast, growth on the C-face happens very quickly, even at relatively low growth temperatures, and more than hundreds of graphene layers can easily be formed. On the Si-face, an interface layer between the substrate and the first EG monolayer is formed during growth, which is structurally similar to monolayer graphene, but contains a large percentage of C atoms bound to the Si atoms below (Figure 2.2).

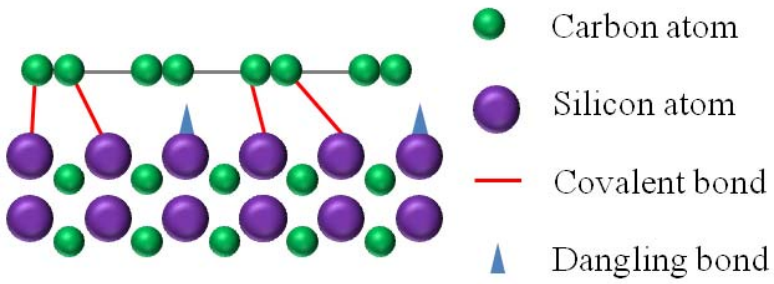

Figure 2.2. The structure and bonding of the buffer layer and the SiC substrate.

Epitaxial graphene monolayers form on top of the interface layer and are intrinsically heavily n-doped to a level of $n \sim 10^{13}$ cm^{-2} [41]. No such interface layer is present on the C-face, which results in EG with a reduced carrier density of $n \sim 10^{12}$ cm^{-2} [42]. As a result of the reduced carrier density, graphene grown on the C-face of SiC substrates exhibits a significantly larger mobility than similar films produced on the Si-face [39]. For this reason, the initial investigations of EG electronic devices were focused on the C-face material. Unfortunately, high-quality monolayer or even few-layer graphene has been exceedingly difficult to produce at a large scale on the C-face, so most EG research is based on results obtained for Si-face growth. In this work, the majority of the electrical measurements were performed on EG produced on the Si-face of semi-insulating *4H*-SiC substrates.

In order for one EG monolayer to form on the SiC substrates, the carbon contained in 3.14 SiC bilayers must be liberated [43]. This is accomplished by heating the substrate to temperatures greater than 1200 °C in vacuum, which allows the Si atoms to preferentially sublime from the SiC bulk. The rate that the Si sublimes from the SiC substrate can be controlled by the temperature or by varying the partial pressure of the Si

in the surrounding environment via confinement or gas overpressure. As a result of differences between growth chambers, such as dimensions, temperature control, and internal materials, EG grown with identical recipes (i.e., time, temperature, pressure) in different tools is expected to vary in both morphology and quality [38, 44, 45].

Before graphitization is performed, the SiC substrate must be flattened to remove severe CMP damage imparted by the SiC manufacturer during wafer preparation. A variety of ways exist in which this can be accomplished, but hydrogen etching is widely used by EG researchers to achieve a smooth surface before graphitization. At elevated temperatures in an environment of molecular hydrogen (H_2), atomic hydrogen can be liberated that is free to react with both the Si and the C in the SiC substrate. Atomic hydrogen forms gaseous silane with the Si atoms and gaseous hydrocarbons with the C atoms, all of which can be simultaneously pumped out of the system. By running the process for a long enough period of time, the uneven surface of the SiC can be smoothed and prepared for graphitization. In addition, at the temperatures required for hydrogen etching, surface contaminants or oxides can be removed to obtain a pristine SiC surface. The surface revealed after hydrogen etching is composed of regular steps and atomically-flat terraces, which are a result of the miscut of the SiC wafer, that range in height from half to several unit cells of the SiC. During graphitization, these steps and terraces are often found to change in shape, uniformity, and dimension as a result of step bunching [46], with many terraces spanning several microns in width.

The terrace structure of SiC has a profound effect on both the thickness and the electrical characteristics of the EG. At a particular SiC surface step, Si atoms can sublime more easily, and regions of thicker graphene are often found in these areas. The overall

structure of the EG on the SiC surface is a continuous film with thicker regions, usually bilayer or trilayer, near the step edges. In the context of patterning electrical devices, the placement of such structures is a crucial parameter in obtaining high charge carrier mobility. Namely, if part of the conducting graphene channel crosses a step edge, additional sources of extrinsic scattering are present that can degrade the mobility. The scattering that occurs near the step edges is attributed to trapped Si atoms between adjacent graphene layers, or between graphene and the SiC substrate, that form as a result of enhanced Si sublimation at these sites [47]. Such scattering can be minimized by orienting the graphene devices along, rather than across terraces, or by designing the device such that the dimensions are smaller than the size of a single terrace, thereby confining the graphene to a particular atomically-smooth region.

To perform the hydrogen-etching and graphitization procedures, a commercial radio-frequency induction furnace was procured for the Institute of Electronics and Nanotechnology (IEN). The furnace was built to custom specifications by CVD FirstNano to ensure that the system could withstand the high level of temperatures required for the graphitization process. Specifically, all of the internal components of the system were made of graphite, which can withstand heating up to 3675 °C. The system was composed of a quartz tube surrounded by copper coils, and the temperature was controlled by an RF power supply capable of inductive heating up to 2500 °C. Accurate temperature determination was provided by two pyrometers, one that read temperatures less than 550 °C and the other that read temperatures in the range 550-2500 °C. The pyrometers were located outside of the chamber and focused on the graphite platen (sample holder three inches in diameter) inside the chamber via the two viewports

(Figure 2.3). The system contained three gas inlet ports into the chamber that were controlled by separate mass flow controllers for accuracy. Chamber pressures as low as $P = 10^{-6}$ Torr were achievable with the dual roughing and turbo pumps installed on the system. All the EG samples used in this research were produced in the described system.

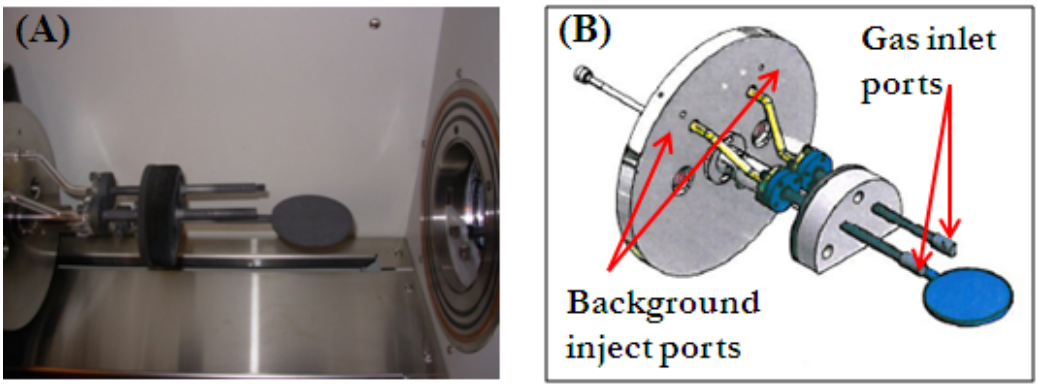

Figure 2.3. CVD FirstNano Graphene Furnace. (A) A side-view of the chamber door with the gas inlet ports and sample platen shown. (B) A schematic of the chamber door showing the location of the background and gas inlet ports above the sample platen.

2.2 SURFACE PREPARATION OPTIMIZATION

Semi-insulating, on-axis, *4H*-SiC substrates were obtained in the form of three-inch wafers from Cree, Inc. The wafer was diced into 3.5 mm x 4.5 mm pieces for processing. The as-received wafers were provided with an epi-ready Si-face surface, and both the Si-face and the C-face were chemically-mechanically polished (Figure 2.4).

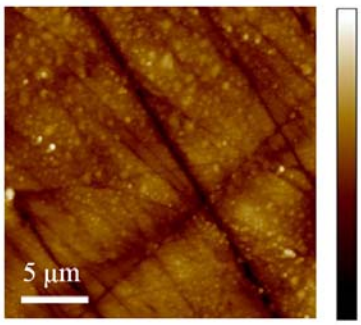

Figure 2.4. AFM image of the as-received Si-face *4H*-SiC substrates showing CMP damage. Gradient scale bar corresponds to a 10-nm height variation.

The optimization of the hydrogen-etching procedure was performed first to remove the CMP damage and obtain the characteristic stepped surface of the SiC substrates. Before loading the samples into the graphene furnace chamber, sonication was performed on the samples in three individual solutions of acetone, methanol, and isopropanol for five minutes each to remove the adsorbates and particles imparted to the substrate surface during the wafer dicing. Multiple samples were then loaded simultaneously into the graphene furnace during each process run, with different polar faces of the SiC substrate exposed. This was performed so that the hydrogen etching procedure for each polar face could be accurately determined. The C-face was expected to be significantly rougher, and as a result, would require more hydrogen etching than the Si-face, which was exposed to an extra epi-ready process by Cree, Inc. The hydrogen-etching recipe was composed of four major variables: temperature, chamber pressure, H_2 and argon (Ar) gas flow/gas mixture, and process time. Information from the EG growth literature [43-45, 48] provided a range of settings for each of the four variables, all which were successful for various SiC substrates and furnaces (Table 2).

Table 2. Standard variables of the hydrogen-etching recipe for SiC surface preparation.

	Variables from Literature	**Experimental Variables**
Temperature (*T*)	1400-1700 °C	1400 °C
Pressure (*P*)	760 Torr (1 atm)	4-760 Torr
H_2 Gas Flow/Mixture	1000 sccm, 5% H_2	200 sccm, 5% H_2
Process Time (*t*)	15-30 min.	30-120 min.

The efficacy of the hydrogen-etching process was determined by AFM imaging of the sample surfaces both before and after the furnace run (Figure 2.5 A). For the Si-face, sufficient hydrogen etching was achieved with T = 1400 °C, P ~ 4 Torr, a gaseous

environment of 200 standard cubic centimeters per minute (sccm) of H_2 and 3800 sccm of Ar, and t = 30 minutes (min). The surface morphology was composed of terraces 2-5 μm in width and 2.5 nm in height (i.e., two SiC bilayers). At higher process pressures, the surface was composed of both macro and microterraces that were detrimental to the electrical conductivity and therefore undesirable (Figure 2.5 B).

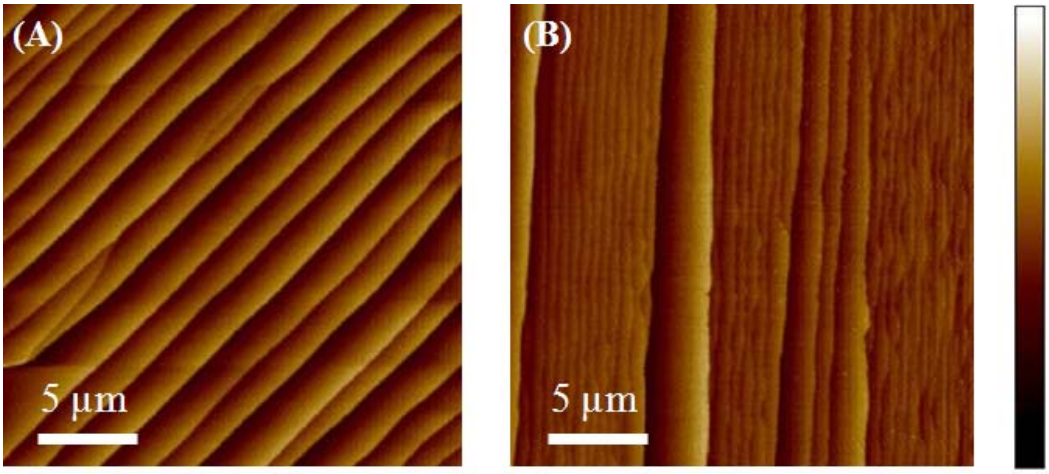

Figure 2.5. The results of the hydrogen etching on *4H*-SiC (0001). (A) Hydrogen etching at *P* ~ 4 Torr. (B) Hydrogen etching at atmospheric pressure. Gradient scale bar corresponds to a 10-nm height variation.

For the C-face hydrogen etching, the process time had to be extended from 30 min. to 120 min. before the terrace structure of the SiC surface was observable. The surface morphology obtained was significantly different than that found on the Si-face, namely the terraces did not possess straight edges and many particles were visible on the surface even after repeated liquid solvent cleaning (Figure 2.6). The increase of the process time and the gas flow did not produce improvements in the surface morphology, and any increase in the temperature led to the premature graphitization of the samples.

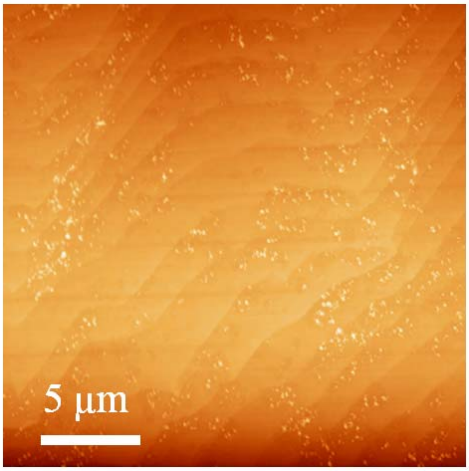

Figure 2.6. The result of the hydrogen etching for 120 min. on the C-face of *4H*-SiC substrates.

2.3 EPITAXIAL GRAPHENE GROWTH OPTIMIZATION

Graphitic bonds are known to form on the surface of the SiC substrates [10] at temperatures as low as 1000 °C in ultrahigh vacuum (UHV), but temperatures greater than 1250 °C are required to form carbon layers with a graphene structure [48, 49]. The initial growth experiments for electronic-grade EG used UHV pressures, but the material was found to exhibit a "swiss cheese" morphology in which numerous pits or voids free of graphene were formed. The graphene grain size was found to be less than 200 nm [50-52] for the samples produced with the UHV method. New approaches based on the growth of graphene at higher pressures, or in an overpressure of Ar or Si, led to continuous, smooth films of EG that extended over large-area SiC substrates and exhibited larger grain sizes [42, 45]. The initial parameters for the graphitization process used in this work were obtained from these literature sources (Table 3), but the resulting graphene was expected to be slightly different as a result of discrepancies in the size of the furnace chamber and the accuracy of the pyrometers monitoring the temperature.

Table 3. Standard variables for the graphitization of SiC substrates.

	Standard Variables from Literature	Experimental Variables
Temperature	1200-2000 °C	1200-2100 °C
Pressure	10^{-3}-750 Torr	~ 4 Torr
Process Time	15-30 min.	1-10 min.

The growth experiments based on the parameters listed in Table 3 were performed with both of the polar faces of the SiC substrates exposed. The pressure was kept at a constant value during the experiments, but the temperature and the soak time at the desired temperature were varied. The optimized hydrogen-etching procedure for each particular polar face was performed before the graphitization, and the samples were not exposed to atmosphere between the two process steps (i.e., both the hydrogen etching and the graphitization were performed in the same chamber). Argon-assisted cooling was used to bring the furnace chamber temperature down to 700 °C after the hydrogen etching at 1400 °C, followed by a fast temperature ramp (~ 120 °C/min) to the desired graphitization soak temperature. The samples were then allowed to graphitize for various amounts of time without any external gases present inside the furnace chamber.

To determine the quality of the EG produced on the different polar faces of the SiC substrates, four distinct characterization procedures were performed on each sample. The structural characterization included AFM imaging and Raman spectroscopy, while the electrical characterization was based on four-point measurements in both the van der Pauw and the Hall configurations. These characterizations were repeated after the growth of all the produced samples in order to ensure process control and repeatability.

For structural characterization, AFM imaging was used to observe the morphology of the sample, including the terrace size and uniformity, and the presence of

any pitting in the material. In addition, the AFM imaging served to aid in determining the angle of the substrate terraces with respect to the sample edge (Figure 2.7). This was an important metric to consider before device fabrication; as mentioned in Chapter 2.1, the direction of the current flow with respect to the terraces (i.e., along or across the substrate step edges) can influence the electrical conductivity. In order to determine how accurate a local AFM scan (20 x 20 μm^2 region) was in comparison to a global view of the entire sample (3.5 x 4.5 mm^2), multiple smaller regions were sequentially scanned and then patched together to give a view of the full sample surface after graphitization. The results of multiple analyses of this type proved that the terrace angle determined from a local scan was constant across the entire sample surface.

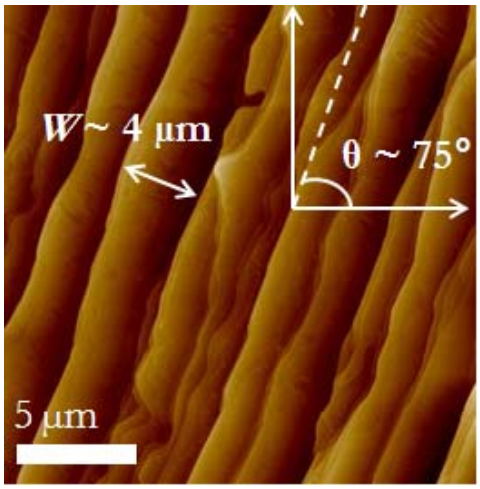

Figure 2.7. AFM image of a 20 x 20 μm^2 region after graphitization of the Si-face of *4H*-SiC substrates. The average size of the terraces can be measured, as well as the angle the terraces make with the edge of the sample.

Raman spectroscopy was used to estimate the thickness and the disorder of the produced EG. The Raman spectrum of graphene is composed of three distinct peaks: the 2D-peak (~ 2690-2760 cm^{-1}), which signifies strain, thickness, and multilayer stacking,

the D-peak (~ 1350-1370 cm^{-1}), which signifies disorder, and the G-peak (~ 1580-1600 cm^{-1}), which also signifies strain in the material. By analyzing the position and the shape of the 2D-peak, the graphene thickness can be estimated. Two general methods are used to characterize this peak: to determine the 2D-peak position and full-width at half-maximum [53], or to fit the 2D-peak with one or more Lorenztians [54]. The determination of the graphene thickness of the samples presented in this research was based on the latter method.

For the electrical characterization of the AG graphene, four-point testing was performed at room temperature in the Hall and van der Pauw configurations with and without the application of an external magnetic field, respectively. The van der Pauw method [55] was used to determine the sheet resistance (R_S) of the graphene, as this technique is useful for thin, conducting samples of arbitrary shape. Eight individual measurements were performed, whereby current (I = 10 nA) was applied to one edge of the sample and the voltage (V) was measured across the opposite edge. The resistance (R) for each measurement can be calculated from

$$R_{12,34} = \frac{V_{34}}{I_{12}}, \tag{2.1}$$

where I_{12} represents the current flowing between the electrodes labeled one and two, and V_{34} represents the voltage measured across the electrodes labeled three and four. Four resistance measurements of this kind were then used to determine the horizontal and vertical resistance components separately according to

$$R_{vertical} = \frac{R_{12,34}+R_{34,12}+R_{21,43}+R_{43,21}}{2} \tag{2.2}$$

$$R_{horizontal} = \frac{R_{23,41}+R_{41,23}+R_{32,14}+R_{14,32}}{2}. \tag{2.3}$$

The combination of Equations 2.2 and 2.3 according to

$$\exp\left(\frac{-\pi R_{vertical}}{R_S}\right) + \exp\left(\frac{-\pi R_{horizontal}}{R_S}\right) = 1 \quad (2.4)$$

was then used to obtain the sheet resistance of the EG. Once R_S was determined, an external magnetic field of 3200 Gauss was applied to the sample, and a slightly modified van der Pauw orientation, the Hall configuration, was used to obtain a set of eight voltage measurements. For each voltage measurement, the polarity of the magnet was switched so that two measurements could be used to calculate

$$V_{13} = V_{13}(Positive\ Polarity) - V_{13}(Negative\ Polarity)\ , \quad (2.5)$$

and allow for the determination of the Hall voltage (V_H) according to

$$V_H = \frac{V_{13}+V_{24}+V_{31}+V_{42}}{8}\ . \quad (2.6)$$

The carrier density was then obtained with the result of Equation 2.6 according to

$$n = \frac{IB}{q|V_H|}\ , \quad (2.7)$$

where the magnetic field (B) was measured in Weber/cm^2. The combination of the carrier density and the sheet resistance allowed the mobility to be calculated from

$$\mu = \frac{1}{qnR_S}\ . \quad (2.8)$$

According to the Raman spectroscopy and the electrical testing, the graphitization of the SiC substrate for either the Si-face or the C-face was not complete across the entire sample surface at temperatures below 1600 °C, regardless of the soak time. The graphene growth is known to nucleate from pinholes or screw dislocations in the SiC substrate [56, 57], so the assumption was made that some regions of graphene were produced near these sites, but a continuous film across the entire SiC substrate was not obtained in the temperature range 1200-1500 °C. At temperatures greater than 1800 °C, pinholes began to form on both the Si-face and the C-face graphene, and the density of the pinholes

increased as the growth temperature approached 2100 °C (Figure 2.8). The lack of complete graphene growth at lower temperatures, and the appearance of pinholes at higher temperatures, can be understood by considering the mechanism of epitaxial graphene formation. Epitaxial graphene is thought to form at screw dislocations in the SiC substrate [56, 57]; graphene grows out from these regions and eventually forms a continuous film across the larger substrate surface. At lower temperatures, the graphene growth resembles islands of graphene centered on the screw dislocations. At higher temperatures, the sublimation rate at these dislocations is so rapid that holes in the substrate form as excessive amounts of silicon are released from the substrate. Therefore, an optimal graphene growth window of 1600-1800 °C was determined. To further optimize the growth parameters, the sheet resistance as a function of the growth temperature was analyzed. The data revealed that for growth temperatures of less than 1800 °C, the resistance of the EG was significantly larger than that predicted in the literature. This result suggested that the continuous growth of the graphene across the entire SiC substrate may not have yet been complete.

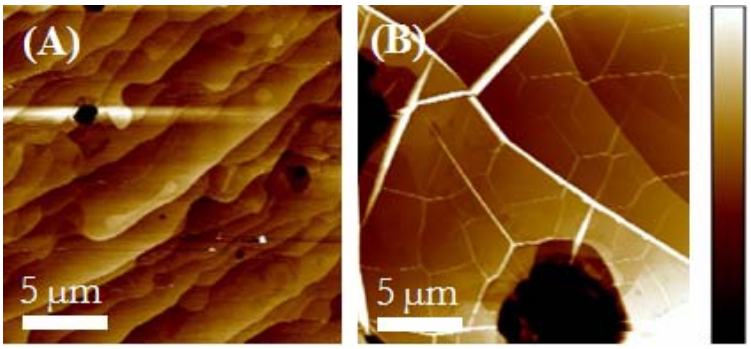

Figure 2.8. AFM scans revealing the presence of pits in the EG samples at growth temperatures greater than 1800 °C. (A) Graphene produced on the Si-face. (B) Graphene produced on the C-face. The scale bar corresponds to a 10-nm height variation.

For the Si-face EG grown at 1800 °C for 10 min., a range of sheet resistance values of R_S = 500-1200 Ω/□ was determined, with the corresponding carrier densities in the range $n = 10^{12}$-10^{13} cm^{-2}. These results agreed quite closely with what has been found in the literature for Si-face EG [58, 59]. The AFM imaging revealed the characteristic structure of the graphene grown on SiC (0001) (Figure 2.9). The Raman spectra revealed mostly monolayer graphene across the entire sample surface, with small regions of bilayer and trilayer graphene present near the step edges (Figure 2.10). The D-peak related to disorder was barely visible outside of the spectrum noise for most monolayer regions, so a low level of disorder was assumed in the produced EG.

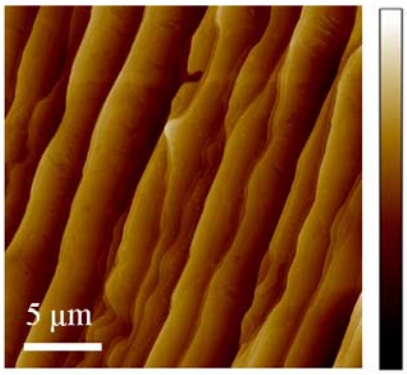

Figure 2.9. AFM image of EG on SiC (0001). Gradient bar corresponds to a 15-nm height variation.

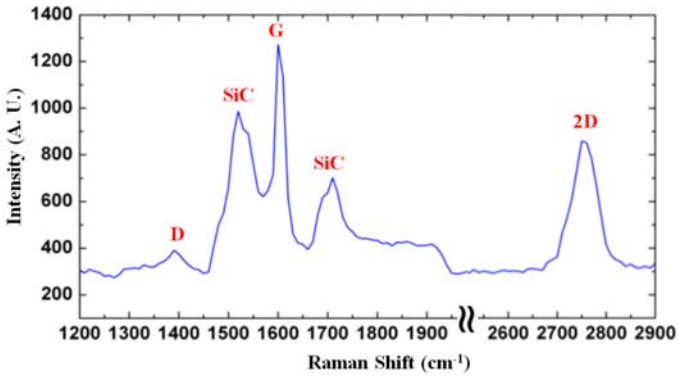

Figure 2.10. The Raman spectrum of EG on SiC (0001) with the graphene and SiC peaks labeled.

For the C-face EG, as expected, the sheet resistance was ~ 10 times smaller than that of the Si-face EG produced with the same growth recipe. Unfortunately, the structure and the thickness of the EG produced on the C-face were undesirable. C-face EG is known to form quite quickly, and monolayer regions of C-face EG can be nearly impossible to obtain. From the Raman spectroscopy, the C-face graphene thickness was estimated to be more than 10 layers thick, and possibly as thick as 100 layers. The spectra obtained from the Raman spectroscopy also revealed an extremely large disorder-induced D-peak that was present in all of the C-face EG samples. In addition, the AFM analysis revealed the characteristic "puckers" or "giraffe stripes" across the sample (Figure 2.11). These puckers are attributed to a thermal mismatch between the SiC substrate and the graphene [43], although no clear consensus has yet been reached as to why this occurs only on the C-face graphene. Although the graphene is found to be continuous over the puckers [56, 60], such large disruptions (> 10 nm) in the surface of the EG are expected to be detrimental to device fabrication and electrical testing.

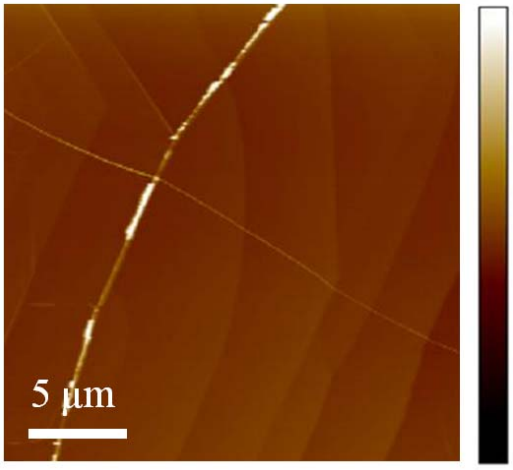

Figure 2.11. AFM image of the graphitized C-face of the *4H*-SiC substrates. The "puckers" or "giraffe stripes" are clearly visible across the multilayer graphene. The gradient scale bar corresponds to a 15-nm height variation.

In addition, the multilayer nature of the EG produced on the C-face leads to problems during transistor operation. The contact electrodes are expected to only make contact with the first few upper layers of the EG, so there is no way to probe the electrical characteristics of the most highly-doped monolayer closest to the SiC substrate. Top-gated transistors must be used for the device characterization because the SiC substrate does not provide a dielectric layer, such as that found on SiO_2/Si substrates. As a result of screening, the top gate cannot accurately control the graphene monolayer closest to the SiC substrate through the stack of multilayers [61]. Because of the challenges associated with the C-face EG, the remainder of this research was focused on the Si-face EG only.

In summary, the optimization of both the hydrogen-etching process to remove the CMP damage from the as-received wafers, and the graphitization of both the polar faces of the SiC substrates have been presented. Four distinct characterization procedures were used to determine the quality of each EG sample: AFM imaging, Raman spectroscopy, the van der Pauw determination of the sheet resistance, and the Hall effect determination of the carrier density. Both the structural and the electrical characteristics of the samples produced in this work agreed well with what has been presented in the literature, therefore a robust process for producing EG has been achieved in this portion of the work. Although the graphitization was possible for both of the polar faces of the SiC substrates, the subsequent research to be presented herein makes use solely of the Si-face EG for electrical measurements because of the limitations encountered by the C-face EG.

CHAPTER III – SIZE-DEPENDENT CONDUCTIVITY OF EPITAXIAL GRAPHENE NANORIBBONS

3.1 PROCESS DEVELOPMENT

In order to obtain electrical measurements of the epitaxial GNRs, the process flow for device fabrication had to be established and optimized. The process flow for creating epitaxial GNRs from the Si-face samples produced in Chapter II was a complex series of both photolithography and e-beam lithography, e-beam evaporation of metal films and oxide, plasma etching, and both AFM and scanning electron microscope (SEM) imaging to confirm the process efficacy.

3.1.1 Layer 1 – Contact Electrodes

After the sample growth and characterization, photolithography was used to pattern the contact electrodes for electrical testing. The designed photomask allowed for the patterning of multiple four-pad devices (8-24 devices) across each 3.5 mm x 4.5 mm graphitized sample. The four-pad configuration was selected to provide for a robust platform for repeated electrical testing. Two different positive photoresists (Shipley) were used in the initial exposure tests: 1827 and 1805. A spin/bake recipe provided by the IEN was used to coat the samples (Table 4).

Table 4. The parameters for applying positive photoresist to the graphene samples.

Spin Speed (rotations per minute)	6000
Spin Time (seconds)	60
Post-Bake Temperature (°C)	115
Post-Bake Time (minutes)	5

The exposure tests of the photoresist-coated samples were performed with a Karl Suss MA6 mask aligner, which uses a 350 watt (W) mercury lamp to provide ultraviolet (UV) light with a wavelength of 405 nm for the resist exposure. Because of the small size of the individual graphitized samples, in contrast to the size of a large wafer which is normally used in exposures of this kind, problems were encountered when using the 1827 resist. The thickness of the 1827 resist was measured to be 2.5 μm using the spin recipe outlined in Table 4, while the 1805 resist was only measured to be 0.5 μm. When spin-coating with a thicker resist on small, square-shaped samples, large photoresist beads were formed at the four corners of the sample. These thicker regions of photoresist were more difficult to fully bake and harden, and therefore, during the exposure process, the samples often became stuck to the photomask itself. The result was an inaccurate exposure and frequent scratching of the photoresist or misalignment of the Layer 1 pattern. To alleviate these problems, the 1805 photoresist was used in an identical spin-coating and exposure process, and the resulting pattern exposure was successful. The alignment gap during exposure was set to 50 μm to ensure that the samples would not stick to the photomask, and the exposure was set for 10 sec. total time. The development of the photoresist was performed in a solution of MF 319, a commercially-available photoresist developer. Directly after exposure, samples were placed in MF 319 and slightly agitated for 1 min., and then rinsed with deionized (DI) water for 30 sec. The samples were then imaged with an optical microscope to determine the exposure and development efficacy, and to check for proper pattern alignment on the sample surface.

3.1.2 Contact Electrode Metallization

After patterning of the contact electrodes, the samples were directly loaded into one of two e-beam metallization chambers, the CVC E-beam Evaporator or the Denton Explorer Evaporator. The systems were pumped down to a pressure of $P \sim 10^{-6}$ Torr before beginning the metallization process to promote high-quality film deposition and to remove any contaminants from the chamber. The metal stack selected for the contact electrodes was a seed layer of 20 nm of titanium (Ti) and 80 nm of gold (Au). Titanium was selected as the seed layer to promote adhesion between the graphene surface and the Au used for electrical contact. The two separate film depositions were performed sequentially without any sample exposure to atmosphere. After the metallization, the samples were placed in a heated solution (120 °C) of 1165, a commercially-available photoresist stripping solution that selectively removes the photoresist and the metal film atop it from those regions that were not exposed during the Layer 1 photolithography. Upon removal from the heated 1165 solution, the samples were cleaned with acetone, methanol, and isopropanol to remove all photoresist residue and any excess metal.

During the initial exposure and metallization experiments, problems with metal adhesion became apparent after the samples were imaged with the optical microscope. Large areas of metal appeared to remain intact after the liftoff procedure, but the smallest features were easily removed and thereby made the patterned devices impossible to use for nanoribbon fabrication. A careful study of the sample surface directly after exposure and before metallization was then performed on subsequent samples, whereby the exposed and developed pattern regions were probed with a Nanospec Refractometer to determine the presence of any resist residue. The presence of trace amounts of resist

residue after development necessitated multiple trials of various exposure and development times in an attempt to remove all photoresist from the patterned region before metallization. A successful combination of exposure and development time capable of removing the photoresist residue was not achieved; with too much exposure or development time, the patterns became much larger than designed and led to the merging of the individual features necessary for nanoribbon device fabrication.

After the unsuccessful exposure and development experiments, a plasma process was designed to remove trace amounts of photoresist without inadvertently etching the graphene surface. Previous experimental work detailing the improvement in adhesion between graphene and contact metals after a surface "wetting" process was the basis for this process development [62]. The samples were placed in a Vision Reactive Ion Etcher (RIE) system directly after Layer 1 exposure and development, and subjected to a brief, low-power oxygen (O) plasma to roughen the graphene surface without completely etching the exposed graphene. The Nanospec Refractometer measurements obtained before and after the plasma treatment revealed that the process was successful in removing all trace amounts of the photoresist from the patterned regions while leaving the graphene below intact. The subsequent metallization and liftoff of the samples exposed to the wetting process provided 100% yield of the designed devices.

Once the metallization and liftoff process was successfully optimized, AFM imaging was performed on the local graphene regions that would be subsequently used for nanoribbon fabrication. The purpose of the AFM imaging was two-fold: to determine the presence of photoresist residue that could be detrimental to electrical characterization, and to determine the quality of the graphene region by detecting the SiC substrate step

edges or any areas of varying graphene thickness. A significant amount of photoresist residue was found during the initial AFM imaging of trial samples (Figure 3.1 A). Photoresist can act as a p-type dopant for graphene, and therefore must be removed before nanoribbon fabrication to obtain a pristine graphene surface for electrical testing [12]. The photoresist residue was removed by placing the samples into the graphene furnace and performing a low-temperature anneal (T = 330 °C) in Ar (3800 sccm) and H_2 (200 sccm) for 3 hours. A plasma process was not selected for the photoresist residue removal because the graphene could be inadvertently etched or damaged by the energetic ions. The AFM imaging performed both before and after the low-temperature anneal revealed the removal of the photoresist residue in the graphene regions of interest (Figure 3.1 B).

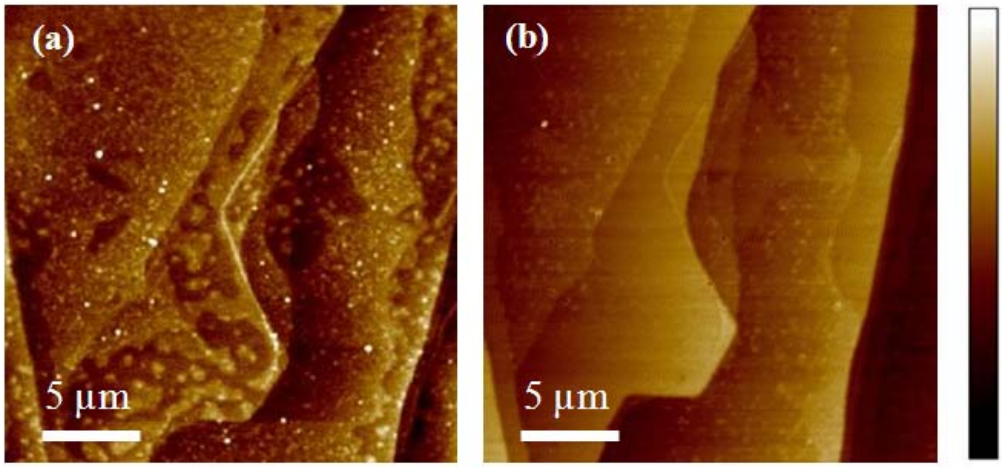

Figure 3.1. AFM images revealing the efficacy of the low-temperature photoresist residue anneal. (A) The graphene region directly after metallization and liftoff. (B) The same graphene region after the Ar/H_2 anneal. A significant improvement in the surface roughness and the removal of the photoresist residue is apparent. The gradient scale bar represents a 15-nm height variation.

3.1.3 Layer 2 – Nanoribbon Fabrication

The fabrication of the epitaxial GNRs was accomplished with the JEOL JBX-9300FS e-beam lithography (EBL) tool. The samples were spin-coated with the negative-tone e-beam resist HSQ on a custom-designed spin chuck fabricated to provide a high level of vacuum for small sample sizes. A baseline spin and bake recipe for HSQ provided by the IEN staff was used to coat the samples (Table 5).

Table 5. The spin and bake parameters for the negative-tone e-beam resist HSQ.

Spin Speed (rotations per minute)	5000
Spin Time (seconds)	60
Post-Bake Temperature (°C)	180
Post-Bake Time (minutes)	3

The EBL process was performed with an e-beam current of I = 2 nA and a base dose for the HSQ resist of 1050 micro-Couloumbs per unit area ($\mu C/cm^2$). The base dose had been optimized by the IEN staff for the exposure of large-area HSQ regions, but the GNRs of different widths and lengths had to be exposed with varying dosages to ensure proper exposure. A careful study of various e-beam dosages with a range of GNR line widths and lengths was performed, whereby numerous feature sizes were exposed, developed, and then subsequently measured with the SEM (Figure 3.2). The development process was performed in three separate solutions, slightly agitated, to ensure the full removal of any HSQ residue: 70 sec. in MF 319, 60 sec. in a dilution of MF 319 and DI water (1:10), and 60 sec. in DI water. This study allowed for the determination of a dosage chart for epitaxial GNR exposures (Table 6).

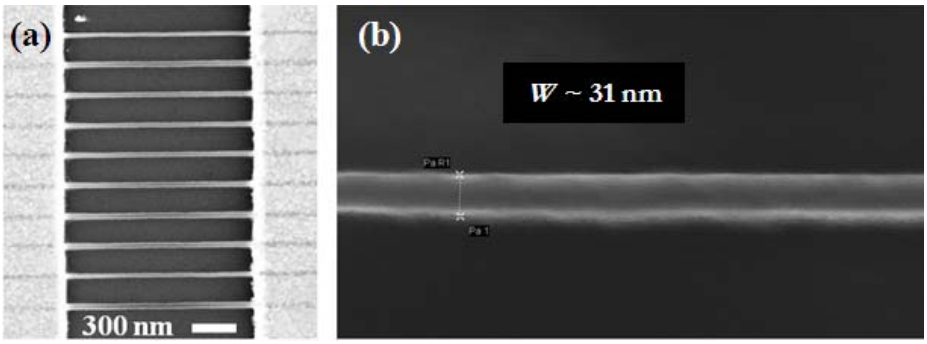

Figure 3.2. SEM images of the exposed epitaxial GNRs. (A) 10 parallel GNRs 1.5 µm in length and designed to be 30 nm in width (B) High-resolution image of a single GNR and the corresponding width measurement of *W* ~ 31 nm.

Table 6. E-beam lithography dosage chart for epitaxial graphene nanoribbons.

Designed Nanoribbon Width (nm)	EBL Dosage (µC/cm^2)
10-20	4200
30-40	3150
50-70	2625
80-100	2100
All larger feature sizes	1575

After the exposure and development of the epitaxial GNRs, a plasma etch process was optimized to transfer the pattern into the graphene sheet and remove the excess graphene not coated by the HSQ. The samples were loaded into the STS SOE chamber, an inductively-coupled plasma system capable of a high level of control of both the power and the direction of the energetic ions through the use of two separate power sources. Argon was selected as the plasma species to avoid any unintentional doping of the GNR edges by more reactive species, such as oxygen. The etch time was determined by etching large-area EG samples for various amounts of time, and then performing two-point electrical testing to check for conductivity. Once the samples were no longer

conductive, the proper etch time had been achieved. The process parameters for the plasma etch are outlined in Table 7.

Table 7. The graphene etch parameters for the STS SOE.

Pressure (mTorr)	10
Gas Flow (sccm)	Ar (25)
Coil Power (W)	125
Platen Power (W)	50
Etch Time (sec)	10

3.1.4 Oxide Deposition and Etching

The fabrication of top-gated epitaxial GNR transistor devices was accomplished by first depositing a blanket oxide layer over the patterned and etched GNRs produced in Chapter 3.1.3. Although most EG devices are fabricated by depositing the top-gate oxide with an atomic layer deposition (ALD) step, the complexity of developing such a process was beyond the scope of this work. The chemically-inert nature of the graphene surface makes the ALD process difficult to implement; water-based precursors are not able to interact with the graphene surface and the oxide deposition is therefore incomplete or nonuniform [63]. To alleviate this effect, surface treatments or seed layers are generally used in the ALD process for oxide deposition.

Alternately, the e-beam evaporation of an oxide layer can provide a suitable top-gate oxide for electrical testing. After the completion of Layer 2, the samples were loaded into the Denton Explorer Evaporator and pumped down to low pressure ($P = 10^{-7}$ Torr) to promote a high-quality oxide film deposition. Silicon dioxide was selected as the oxide of choice due to the accessibility of the material. Initial electrical testing of the top-gated devices fabricated with a 30-nm thick layer of SiO_2 showed premature gate breakdown;

the Dirac point of the fabricated epitaxial GNR devices was not visible in the gate voltage sweep afforded by such a thin oxide. The SiO_2 thickness was then increased to 100 nm, and the resulting gate voltage sweep of more than 150 V was sufficient for the electrical testing of the epitaxial GNR devices.

Before the devices could be probed electrically, the SiO_2 covering the contact electrodes had to be removed so that electrical contact could be made. Although the 100-nm SiO_2 film could be successfully removed by scratching the oxide with the probe tip, such a procedure was harmful to the testing equipment and the contact electrodes. Instead, a standard oxide etch recipe run in the Vision RIE chamber was used to remove the oxide layer in selected regions. Before the etch process, the samples were coated with positive photoresist in the same manner outlined in Chapter 3.1.1. A subsequent exposure using an alternate photomask pattern allowed for the creation of large windows over the metallized contact electrodes. The etch process was then performed on the exposed regions, and the samples were run through a liftoff process identical to that described in Chapter 3.1.2.

3.1.5 Layer 3 – Top-Gate Electrode

Following the oxide deposition and etch step, a third photolithography step and a second e-beam metallization/liftoff process was used to pattern the top-gate electrode. The process parameters of the lithography and the metallization/liftoff were identical to those outlined in Chapters 3.1.1 and 3.1.2. The pattern for the top-gate structure was made up of a contact electrode identical in size to those used for Layer 1, and a thin gate finger that was carefully centered over the GNR region. The width of the gate finger was

designed to slightly overlap the Layer 1 contact electrodes, thereby ensuring that the entire graphene region would be effectively modulated during the electrical testing.

The optimized process flow developed in this section was used to fabricate all of the epitaxial GNR devices used in the remainder of this work. During the size-dependent conductivity study, a device of the type shown in Figure 3.3 was used. Later research focused on the transistor characteristics of epitaxial GNR devices was based on the top-gate design described in Chapters 3.1.4 and 3.1.5. By carefully optimizing the design of the devices, as well as the parameters for each tool and process, a robust platform for the electrical testing of epitaxial GNRs was produced.

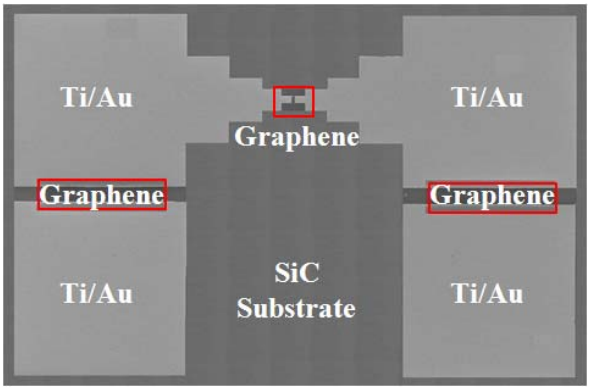

Figure 3.3. SEM image of the optimized EG nanoribbon device used in the size-dependent conductivity study.

3.2 THE SIZE EFFECT IN EXFOLIATED GRAPHENE NANORIBBONS

In order to fully utilize the myriad benefits of EG for future logic devices or electrical interconnects, a clear understanding is required of the limitations faced by the material as the dimensions are scaled below one μm. As discussed in Chapter I, GNRs hold great promise for the future of EG electronics as a result of the ability to induce an

energy gap in the material and improve the switching efficacy of graphene transistors. Unfortunately, during the fabrication of the GNRs, a certain amount of unavoidable LER is imparted to the material that causes the pristine armchair or zigzag edge structure to be effectively wiped out [64]. The major consequence of the LER is a significant degradation of the mobility as the GNR line widths are successively scaled down, although the on-off current ratios of graphene-based transistors have also been shown to decrease as a function of the LER [65]. Theoretical studies based on scattering mechanisms in graphene suggest that for GNR line widths of five nm and below, the carrier mobility degradation is dominated by the LER scattering [65, 66]. In contrast, previous experimental work [67] investigating the size effect in exfoliated GNRs shows that the LER-limited mobility dominates the overall GNR mobility at a significantly larger line width of 60 nm (Figure 3.4). Such a discrepancy between the theory and the experiment suggests that further research is required to fully understand the impact of the LER scattering in lithographically-patterned GNRs.

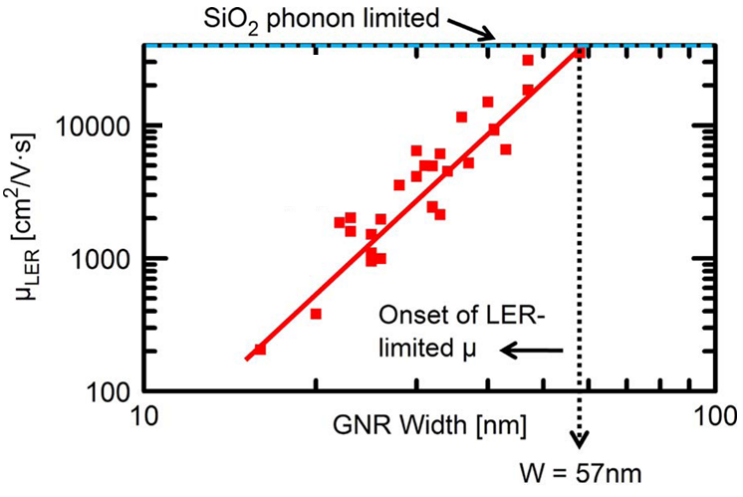

Figure 3.4. The size effect in exfoliated GNRs on SiO_2/Si substrates. Below a line width of $W \sim 60$ nm, the LER-limited mobility is seen to drastically reduce to only 200 cm^2/V-s [67].

The size effect in exfoliated GNRs was found to manifest as a reduction in the mobility from μ = 3000 cm^2/V-s for a one-μm wide ribbon to only μ = 200 cm^2/V-s for a 15-nm wide ribbon [67]. In comparison to these results, a distinct difference in the size effect was expected for epitaxial GNRs, which exhibit variations in the supporting substrate, the substrate morphology, and the intrinsic charge carrier density. Both the supporting substrate and the substrate morphology serve as different scattering sources in EG as compared to ExG on SiO_2/Si substrates. The study of the size effect presented in this chapter was the first to provide a detailed analysis of the impact of both the LER and the substrate morphology on the electrical conductivity of scaled epitaxial GNRs.

3.3 THE SIZE EFFECT IN EPITAXIAL GRAPHENE NANORIBBONS

3.3.1 Experimental Considerations

Before the fabrication of the epitaxial GNRs for the size-dependent conductivity study, the substrate morphology of each as-grown EG sample was carefully determined with a combination of optical and AFM imaging. The clear differences in the terrace size and uniformity observable across the individual samples were partially attributed to the location from which each individual die (~ 3.5 mm x 4.5 mm) was selected from the original SiC wafer. Careful AFM characterization was performed before and after the hydrogen-etching/graphitization processes on individual die procured from various regions of the larger SiC wafer. The imaging results suggested that die selected from regions close to the edge of the three-inch SiC wafer experienced significantly more nonuniform terrace structure. This may have been a result of edge effects and the CMP process performed by Cree Inc. during the wafer preparation.

After the fabrication of the epitaxial GNRs, SEM imaging was performed on each of the individual GNR devices to determine which devices, if any, were patterned across a substrate terrace step. Such devices were expected to behave differently than those devices composed of GNRs that were completely contained within a single SiC terrace due to thickness variations in the graphene near the step edge. The particular device design of multiple GNRs in parallel was selected to average out any small local variations in the line width and the carrier density.

The electrical measurements in this study were obtained with an SRS-830 lock-in amplifier and an excitation current of I = 10 nA. The samples were tested in the ambient environment at room temperature. A four-point measurement mode was used to eliminate the element of contact resistance. Electrical measurements initially obtained in the two-point mode revealed a large variation in the contact resistance across the individual devices on a single sample. This variation was partially attributed to the presence of microscopic photoresist residue and possible poor adhesion between the graphene and the metal stack.

3.3.2 The Size-Dependent Conductivity

The study of the size effect in the epitaxial GNRs was based on the resistivity values calculated from four-point resistance measurements. A range of sheet resistance values (R_S = 500-1150 Ω) of the as-grown EG samples was found before the device fabrication (Figure 3.5 A). Previous work based on sheet resistance measurements of EG had revealed an anisotropic conductance in the graphene as a result of the direction of the current flow with respect to the substrate terraces [47]. No behavior of this kind was

clearly evident in the measurements provided herein (Figure 3.5 A). Although all of the tested samples were graphitized with identical growth recipes, there was unavoidable variability in the final growth results, as was apparent from the variation in the terrace angle and the sheet resistance. The terraces on the SiC substrate were formed during both the hydrogen-etching procedure and the graphitization step; graphitization then proceeded from these terraces and the result was a step morphology over which the graphene was continuous [39]. The terrace angle, width, and height were all heavily dependent on the process conditions [38, 44, 45]. For the size effect study samples, the direction of the terraces with respect to the GNR orientation was distributed between 0^{o}-90^{o}, with clusters at 45^{o} and 80^{o}. After the device fabrication, the size effect behavior was found to fluctuate from sample to sample, even when the GNR orientation with respect to the terrace angle was identical. Three samples with identical terrace angles (45°) exhibited varying size effects (Figure 3.5 B). This suggested that the terrace angle alone could not fully account for the varied behavior of the studied samples.

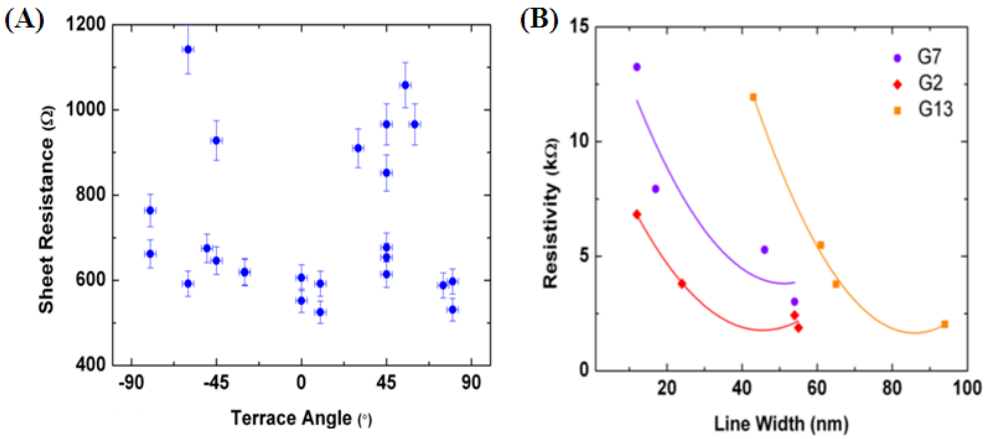

Figure 3.5. (A) Sheet resistance measurements of the as-grown EG as a function of the terrace angle with respect to the sample edges. (B) The size effect behavior for three samples with identical GNR/terrace angle orientation.

The 2D resistivity versus line width for all the studied samples is plotted in Figure 3.6. From this plot, it is evident that the resistivity has increased in comparison to the values obtained for the as-grown graphene sheets (Figure 3.5 A). The rate of the resistivity increase is seen to vary from sample to sample. Some samples exhibit increasing resistivity starting at line widths of 60 nm (similar to exfoliated GNRs), whereas other samples show the onset of this increase at much larger line widths. To determine the reason for this behavior, the individual sample characteristics were considered, including the terrace width and height, and the angle between the GNRs and the substrate terraces. Two extreme cases of the size effect were seen in samples that exhibited a 0° (Sample R4) and 90° (Sample G6) terrace angle with respect to the direction of the GNR current flow. A significant increase in the resistivity of the GNRs in Sample G6 was observed as compared to the resistivity of the GNRs in Sample R4. This directly correlated with the previous work based on the conductance anisotropy in EG, although this behavior was not witnessed for the as-grown samples studied in this work (Figure 3.5 A). This discrepancy again suggested that the terrace angle does play some role in the size effect, but the terrace angle is not the sole source of the conductivity degradation witnessed as the GNR line widths were scaled down.

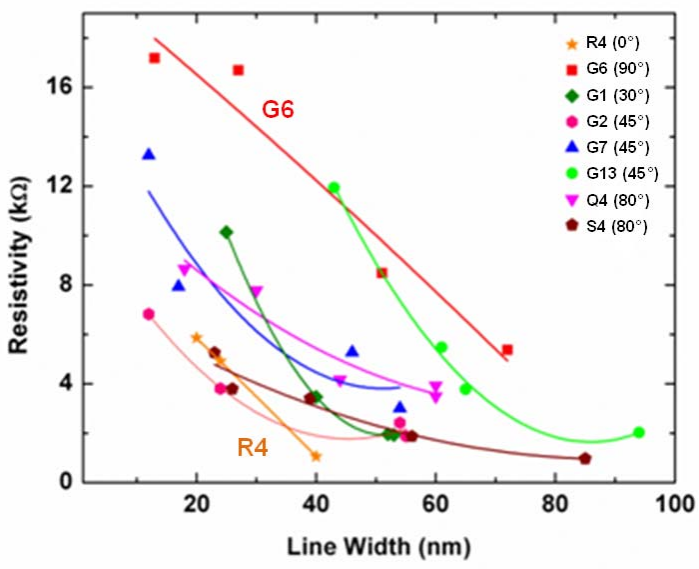

Figure 3.6. Two-dimensional resistivity as a function of the GNR line width is plotted for eight different samples. The sample name and the terrace angle with respect to the GNR orientation are shown in the legend. Samples G6 and R4 are labeled in the figure to highlight the extreme differences in the size effect for these two samples.

To understand the GNR behavior of the various samples, a model for the size effect in the EG was devised. The Drude model was used to calculate the resistivity:

$$\rho = qn\mu_{GNR} \tag{3.1}$$

where q was the electronic charge, n was the charge carrier density, and μ_{GNR} was given by

$$\frac{1}{\mu_{GNR}} = \frac{1}{\mu_{2D}} + \frac{1}{\mu_W} . \tag{3.2}$$

Here, μ_{2D} was the mobility of the 2D graphene (as measured for the AG graphene in the Hall configuration), which included the components of impurity, substrate-phonon, and intrinsic scattering, and μ_W was the size-dependent mobility. The size-dependent component has been shown for exfoliated GNRs [67] to be of the type:

$$\mu_W \propto W^B \tag{3.3}$$

where W was the GNR width and $B \sim 4.3$. Similarly, the size-dependent mobility for the epitaxial GNRs was modeled as

$$\mu_W \propto AW^B \,, \tag{3.4}$$

where A and B were fit constants. A threshold line width (W_{th}) was evaluated so that when $W_{th} = W_{GNR}$, $\mu_{2D} = \mu_W$. The metric W_{th} was meant to represent the GNR line width at which μ_W began to dominate the overall mobility. Thus, W_{th} could be used to judge at what GNR line width a sample would start displaying the width dependence, while the fit constant B could be used to judge the severity of the width dependence.

For a range of samples, an excellent fit between the model and the experimental data was observed (Figure 3.7). Table 8 shows the extracted parameters for the various samples. It can be seen that Sample R4 exhibited a behavior ($B \sim 3.75$) similar to exfoliated monolayer GNRs. In contrast, Sample G6 exhibited an onset of the size effect at a line width as large as 942 nm, and a weaker width dependence of $B = 0.74$. The model suggests that, in general, the earlier the onset of the size effect, given by larger values of W_{th}, the weaker the dependence on W, given by smaller values of B. To explain this behavior, two distinct sources of scattering that contribute to μ_W were defined: the first was "edge scattering" caused by the interaction of the charge carriers with the GNR edges, and the second was "boundary scattering" that occurred at grain boundaries, points of graphene thickness variation, and SiC terrace step edges.

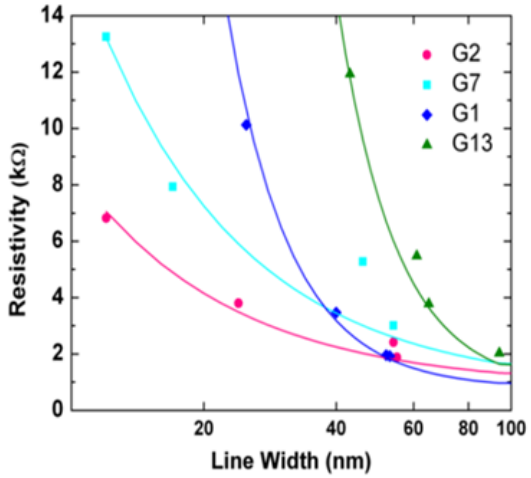

Figure 3.7. The model fit to the experimental data for various size effect samples.

Table 8. The mobility and model parameters of a 50-nm GNR on the samples.

Sample	Terrace Angle (°)	W_{th} (nm)	B	μ_{2D} (Hall)	μ_W (50 nm)	μ_{GNR} (50 nm)	ρ_{GNR} (50 nm)
R4	0	32	3.75	4740	25008	3985	1120
G6	90	942	0.74	2639	218	201	7775
G1	30	66	3.01	3226	1438	995	1995
G2	45	78	1.23	2743	1563	995	1794
G7	45	156	1.28	4373	1180	929	3058
G13	45	79	3.26	1765	380	313	7686
Q4	80	250	1.06	4120	969	784	4045
S4	80	55	2.60	1343	1051	589	1537

The increase in the resistivity of the epitaxial GNRs as a function of the decreased line width depended on the interplay between the edge scattering and the boundary scattering. AFM images of three different samples (R4, G7, and G2) are compared in Figure 3.8. It was observed that Sample R4 had large uniform terraces, with an average terrace width (W_T) of 3.9 μm. Samples G7 (W_T ~ 1.2 μm) and G2 (W_T ~ 1.4 μm) exhibited narrow, nonuniform terraces. For the samples with small, nonuniform terraces, the size effect began to dominate the mobility at larger line widths, as characterized by an

increased value of W_{th}. In addition, the rate of the increase in the resistivity, as characterized by small values of *B*, was found to be weaker for these samples. This may have been due to the fact that the scattering events were dominated by the boundaries, and the reduction of the line width only marginally increased the overall scattering. This was clearly shown in Sample G6, where the width dependence was very weak, suggesting that the boundary scattering was dominating the degradation of the carrier transport and subsequently masking the impact of the edge scattering. In the case of graphene on a flat substrate free of terraces and grain boundaries, the line width scaling will result in increased edge scattering, leading to the predicted ~ W^4 dependence [67] of the resistivity; the onset of the size effect in this case will depend mainly on the LER. Samples R4 and G6 were at the extreme ends of the size effect spectrum, where Sample R4 showed a behavior superior to high-quality exfoliated GNRs and Sample G6 showed an early onset of the width dependence. Most other samples fell between these two extremes.

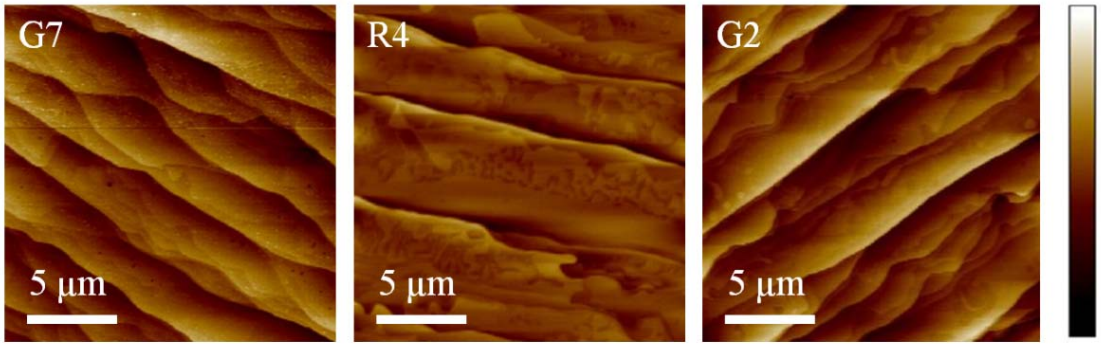

Figure 3.8. AFM images highlighting the substrate morphology differences across the individual samples. The gradient scale bar corresponds to a 10-nm height variation.

In this study, the size effect behavior was shown to have only a weak correlation to the Hall mobility, which was extracted from the large-area EG sheets before GNR device fabrication. It was possible that low resistance regions on the large graphene sheets could provide conduction pathways to the charge carriers and thereby result in a mobility value that did not reflect the microscopic structure of the substrate. Therefore, the terrace morphology and the terrace angle with respect to the patterned GNRs were better metrics to predict the size-dependent conductivity behavior.

The GNRs studied in this work were covered by HSQ during the electrical testing. A study based on HSQ doping of ExG has revealed [68] a predictable shift in the carrier density. Since the doping from the HSQ would be similar for all the GNRs studied in this work, the size effect behavior observed should be a result of the substrate morphology and the edge interactions of the charge carriers in the graphene alone. In addition to the terrace angle and the uniformity, differences in the carrier density between the samples are another possible cause for the variation in the resistivity trends witnessed across the samples. Both the previously published work [39] and the data presented herein show a resistivity difference of less than 3X from the lowest to the highest AG carrier densities measured. Such a variation was much too small to explain the GNR resistivity variation observed from sample to sample, and thus, the observed differences in the resistivity between the samples for the GNR widths studied in this work should come from the edge and boundary scattering, and not from changes in the intrinsic carrier density.

In addition to the charge carrier density variation from sample to sample, it is possible that the charge carrier density can vary within a sample. To find out how this variation can affect the resistivity of the GNRs across a sample, three samples were

fabricated with multiple devices patterned with GNR line widths of 20-30 nm. The resistivity variation of these samples is presented in Figure 3.9 A. The variability in the resistivity for a group of similar line widths was found to be much smaller in comparison to the difference between the AG graphene R_S and the range of the resistivity values found for the GNR devices. The variability measured was also smaller than the rate of the resistivity increase measured as the line width was scaled to less than 100 nm. These results show that the charge carrier density variations within a sample are not significant enough to alter the size effect behavior seen in this study. The mobility of the GNRs on Sample S4 is shown in Figure 3.9 B. This was a moderate-quality sample, and it was chosen to portray the mobility degradation as a function of the GNR line width scaling. It can be seen that for a GNR line width of $W \sim 23$ nm, the mobility has degraded by almost 6X from the as-grown graphene value. For the group of samples studied in this work, the mobility range for a 20-nm GNR was found to be 100-500 $cm^2/V\text{-}s$.

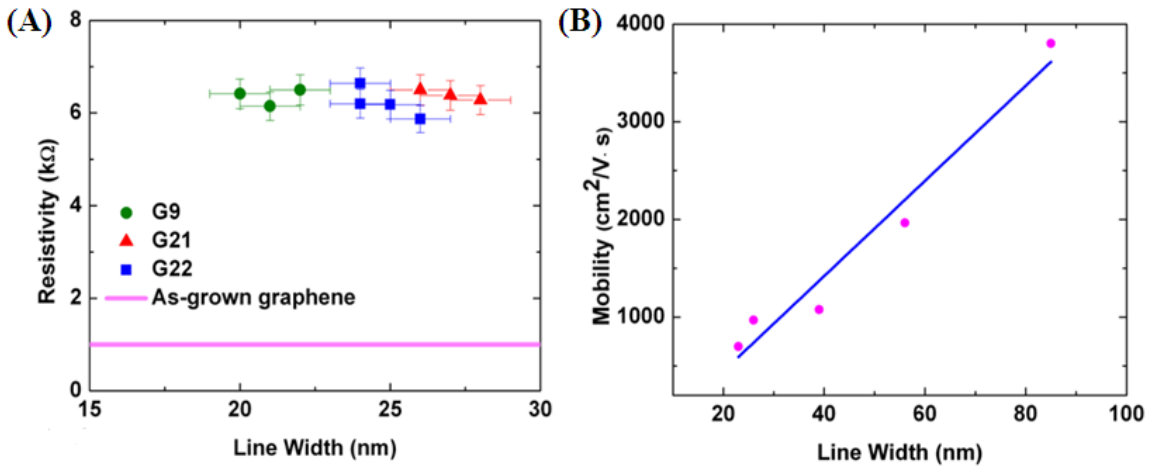

Figure 3.9. (A) Comparison between the as-grown graphene resistivity and the resistivity of identically-sized GNRs on three individual samples. (B) The mobility degradation as a function of the line width scaling on a moderate-quality sample.

In summary, the first experimental evidence of the size effect in epitaxial GNRs on SiC substrates has been shown [69]. The size effect was found to be a function of both the edge scattering from the lithographically-patterned LER and the boundary scattering provided by the unique substrate morphology. A model was derived to explain this sample dependence, and the results of the model suggested that increased boundary scattering dominates for certain samples, thereby leading to an early onset of the size effect. The high-quality samples showed a GNR line width dependence similar to that of exfoliated GNRs, while the low-quality samples showed a weak width dependence.

Although the size effect in epitaxial GNRs has been shown in this study to be detrimental to the conductivity of nanoscale devices, a number of avenues for improvement exist. Further work based on the control of the SiC substrate preparation and the graphitization process may allow for a reduction in the boundary scattering associated with terrace step edges and variations in graphene thickness. Step-free mesas have been successfully produced on SiC substrates [70], and more recent work based on the implementation of a similar process [71] has shown step-free mesas as large as 20 μm. Subsequent graphitization on such large, atomically-smooth regions could possibly eliminate many of the detrimental effects attributed to step-edge boundary scattering, and thereby improve this aspect of the size-dependent conductivity. Such a materials growth-based study is beyond the scope of this work, but the recent results hold great promise for the improvement of the SiC substrate morphology and the alleviation of detrimental scattering sources in GNRs. Furthermore, as will be discussed in the following chapter, the reduction of the influence of the roughened GNR edge can lead to decreased LER scattering and provide a route to high mobility GNRs.

CHAPTER IV – HYDROGENATION OF GRAPHENE NANORIBBON EDGES

As discussed in Chapter III, the LER imparted to the edges of GNRs during patterning and subsequent plasma processing was found to be detrimental to the electrical conductivity. In order to utilize GNRs for logic devices and interconnects at the nanoscale, improvements in the LER are required to retain the superior charge carrier mobility intrinsic to the graphene. In this chapter, a novel method to reduce the influence of the LER is presented, whereby selective regions of the GNRs were functionalized with hydrogen. The expected result was an improvement in the GNR mobility due to the reduced influence of scattering at the GNR edges. In addition, improvements in the size-dependent conductivity were expected.

The functionalization of graphene with hydrogen was first investigated by the University of Manchester group as a way to convert the graphene from a zero-gap semimetal into an insulator [12]. The exposure of ExG to atomic hydrogen resulted in "graphane", an insulating analog to the traditional graphene structure in which the sp^2 bonds are converted to sp^3 bonds, thereby removing the conducting π-bands [12, 72]. True graphane is created only if the hydrogen atoms attach to both sides of the graphene monolayer, a process that is only achievable if suspended graphene is used. If, instead, the hydrogen only bonds to one side of the graphene, the material is known as hydrogenated graphene [73]. In order to attach hydrogen atoms to the graphene lattice, ExG samples were exposed to a low-power hydrogen plasma [12]; the samples were kept away from direct contact with the plasma to prevent any unwanted etching of the graphene film by the energetic ions. The electrical measurements made both before and after the hydrogenation process

revealed significant changes in the electrical transport properties of the graphene. The hydrogenated graphene exhibited a positive shift of V_{Gmin} of more than +50 V, an increase in the resistivity of more than two orders of magnitude, and a decrease in the charge carrier mobility from $\mu \sim 14{,}000$ cm^2/V-s to only $\mu \sim 10$ cm^2/V-s. The hydrogenation process was found to be partially reversible upon annealing at 450 °C in an Ar atmosphere; the samples remained slightly p-doped, and the mobility was only increased to $\mu \sim 3500$ cm^2/V-s, a fraction of the original mobility of the pristine graphene. These results, as well as similar work performed on GNRs [74], reveal that the hydrogenation of graphene is successful in achieving a significant reduction of the graphene mobility in the functionalized regions.

In order to reduce the impact of LER scattering on the electrical transport properties of GNRs, the conducting regions near the edge of the ribbon must be effectively removed to reduce the diffusive scattering encountered by the charge carriers. Because the current processing techniques used to fabricate the GNRs are not able to remove the rough edge regions, the selective hydrogenation of these areas is an attractive, alternative technique. By attaching hydrogen to only the edges of the GNRs, the mobility in these regions is predicted to dramatically decrease, thereby achieving the desired effect of limiting conduction along the rough GNR edge. Theoretical work based on the hydrogenation of wide graphene ribbons in an effort to produce narrow ribbons with smooth edges has conclusively shown that hydrogen atoms will preferentially bind to the exposed carbon atoms at the edge of the graphene [75]. The efficacy of such a process was tested in this work, as the goal of the research presented herein was to allow for the functionalization of only the GNR edge.

4.1 PROCESS DEVELOPMENT

The development and optimization of the process for the hydrogenation of GNR edges was first performed on ExG samples. Because epitaxial GNR devices must be fully fabricated (i.e., addition of the gate oxide and top-gate structure) before conclusive electrical measurements can be made, this platform is less than desirable for use during the process development. In contrast, ExG samples were electrically tested with a back-gate structure. Such an orientation allows for accurate electrical measurements to be made after each step of the process: after GNR fabrication, after the trimming of the HSQ at the GNR edges, and after the hydrogenation of the GNR edges. For this reason, the hydrogenation study was first performed on ExG samples, and then the process was transferred to the EG platform.

The ExG samples were produced with the mechanical exfoliation method: flakes of Kish Grade B graphite were transferred to the surface of 300-nm SiO_2/Si substrates with a piece of generic tape. Before the flaking process, the SiO_2/Si substrates were exposed to a brief oxygen plasma (*Power* = 300 W, t = 2 min.) and a thermal anneal (T = 300 °C, t = 60 min.) to remove any adsorbates and promote adhesion between the graphene and the substrate. The SiO_2/Si substrates were pre-patterned with a photolithography and metallization/liftoff process to provide alignment marks for the accurate determination of the graphene flake locations. After the mechanical exfoliation process, the position of monolayer graphene flakes was determined with an optical microscope (Figure 4.1). Graphene regions (large-area and GNRs) were then patterned following the procedures outlined in Chapter 3.1.3.

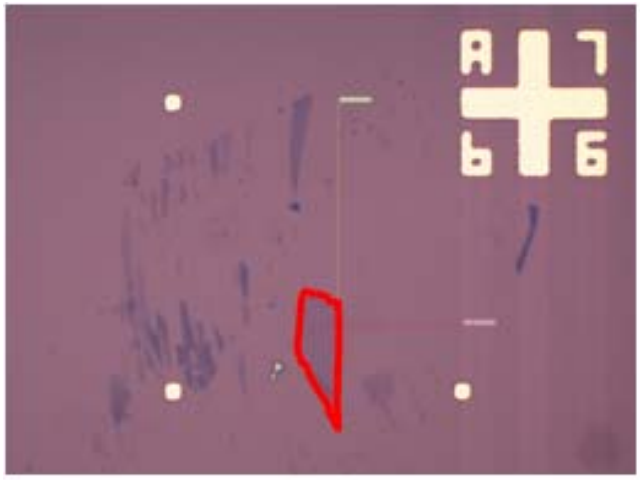

Figure 4.1. An optical image of a monolayer graphene flake (highlighted in red) on the SiO_2/Si substrate. The cross and letters/numerals in the upper right-hand corner are alignment marks used during e-beam lithography to locate the flake for patterning.

The hydrogenation of only the GNR edges required the selective removal of the HSQ thin film atop the graphene. As will be discussed in further detail in Chapter V, HSQ is similar in structure to SiO_2, and therefore wet etching with hydrofluoric acid (HF), a strong etchant for oxides, can be used to remove the HSQ thin film. Because only a small region of the GNR edge was meant to be removed, an extreme dilution of HF had to be used to slow down the etch rate and allow for accurate control of the HSQ removal. A buffered oxide etch solution of ~ 7% HF was diluted repeatedly with DI water to accomplish the desired etch rate control. The exfoliated GNRs were exposed to various dilutions of HF, and then imaged with the SEM to estimate the amount of HSQ removal and thereby extrapolate the etch rate (Figure 4.2). Numerous experiments of this kind were repeated on individual samples, and yielded an ideal etch rate of 0.5 nm/sec with an HF dilution of 0.1%. All further ExG samples used in this study were subjected to the 0.1% dilution of HF for t = 10 sec. to remove ~ 2.5 nm of HSQ on either edge of the GNR. Although the HF etch was isotropic, the thickness of the HSQ etch mask (~ 30 nm)

was sufficiently thick so that the removal of ~ 5 nm of the HSQ laterally still left a thick HSQ film atop the GNRs. This was a key requirement of the trimming process, as the full removal of the HSQ would allow for both the basal plane and the edges of the graphene to react with the hydrogen plasma during the hydrogenation process.

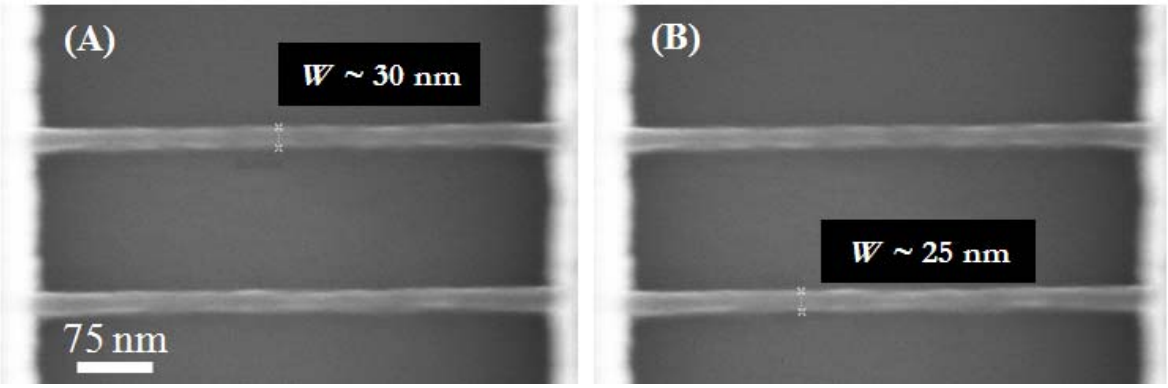

Figure 4.2. SEM images of a 30-nm exfoliated GNR coated with HSQ showing the efficacy of the trimming process. (A) Before trimming, the GNR width is *W* ~ 30 nm. (B) After trimming, the HSQ-coated portion of the GNR has been reduced to *W* ~ 25 nm.

After the HSQ trimming process was optimized, the hydrogenation process was developed by following the experimental variables presented in the literature [12, 74]. The Plasma-Therm SLR RIE was selected for the hydrogenation process due to the ability of the tool to achieve a low level of power while keeping the hydrogen plasma ignited. Because the previous work suggested the use of a remote plasma to avoid any unintentional etching of the graphene, a shield structure was fabricated to mimic the effects of a remote plasma (Figure 4.3). The function of the shield structure was to protect the graphene samples from direct exposure to the energetic ions in the plasma, while still allowing the hydrogen to react with the sample in a diffusive manner through the openings on the sides of the shield. The plasma power was tuned to the lowest

available level (*Power* = 13 W), and the process time was continuously increased from 2 min. up to 60 min. During the development of the hydrogenation process, large-area ExG and EG samples were used to optimize the process parameters and allow for easy characterization via Raman spectroscopy.

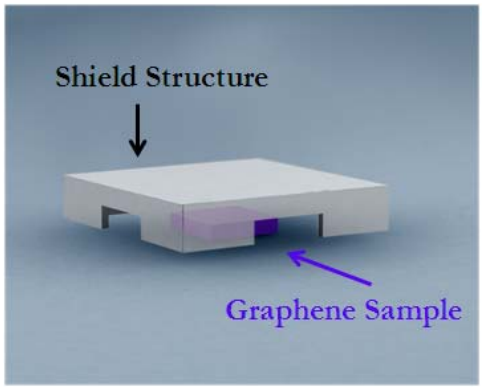

Figure 4.3. Schematic of the shield structure fabricated to protect the graphene from direct exposure to energetic ions during the hydrogenation process.

Raman spectroscopy is widely used as the characterization method of choice in determining the level of hydrogenation of ExG [12, 73, 74]. The hydrogenation process is expected to induce a sharp D-peak near 1342 cm^{-1} as a result of the conversion of the C-C sp^2 bonds to C-H sp^3 bonds [12]. Pristine graphene samples should reveal a minimal D-peak, so the evolution of this particular aspect of the Raman spectrum is a good metric for determining the efficacy of the hydrogenation during the development process. In addition, the evolution of two smaller peaks, D' at 1620 cm^{-1} and D + D' at 2950 cm^{-1}, is expected. The Raman spectra of large-area, monolayer ExG is shown in Figure 4.4. By analyzing the Raman spectra of multiple samples exposed with various experimental parameters, the proper plasma power and process time was determined for the

hydrogenation step. Hydrogenation was found to be effective at a process time of 5 min. for large-area, monolayer ExG. When hydrogenating the edges of the GNRs, the process time was reduced to 2 min. because of the increased reactivity of the GNR edges in comparison to the basal plane [74, 75].

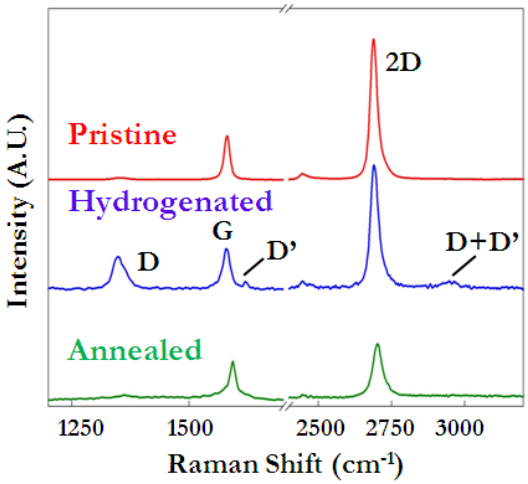

Figure 4.4. The Raman spectra of exfoliated graphene as-fabricated (red), after hydrogenation (blue), and after thermal annealing (green). The hydrogenation process induces the D-, D'-, and D+D'-peaks. Thermal annealing is effective in nearly full removal of the disorder-induced D-peak.

In order to confirm that the electrical transport changes of the hydrogenated GNRs was due to hydrogen attachment and not inadvertent etching of the graphene, a thermal annealing process was also developed to reverse the effects of the hydrogenation. According to previous work [12], the hydrogen attached to the surface of the graphene should be easily removed upon heating in an environment of Ar. The CVD FirstNano graphene furnace was selected as the equipment for the thermal annealing process due to the high level of temperature control afforded by the tool. The hydrogenated, large-area, ExG samples were loaded into the chamber, pumped down to a pressure of $P \sim 600$ Torr, and heated to a temperature of $T = 300$ °C for various amounts of time. The subsequent

analysis of the Raman spectra of the annealed samples revealed that a soak time of 30 min. was sufficient to significantly reduce the intensity of the D-peak (Figure 4.4), although increases in the annealing time did not result in full removal of the D-peak. This may be due to slight disorder induced in the graphene as a result of the plasma exposure.

Similar experiments were performed on large-area EG samples, and a hydrogenation time of 5 min. was found to be sufficient to functionalize the EG. The Raman spectra of the EG samples are shown in Figure 4.5. The presence of the D'-peak was not noticeable due to the SiC peak directly to the right of the G-peak. The D+D'-peak witnessed for ExG was not visible outside of the spectrum noise. The thermal annealing process time of 30 min. was also successful in significantly reducing the intensity of the D-peak, but full removal of the D-peak was not achieved, suggesting slight disorder induced in the EG during the plasma exposure.

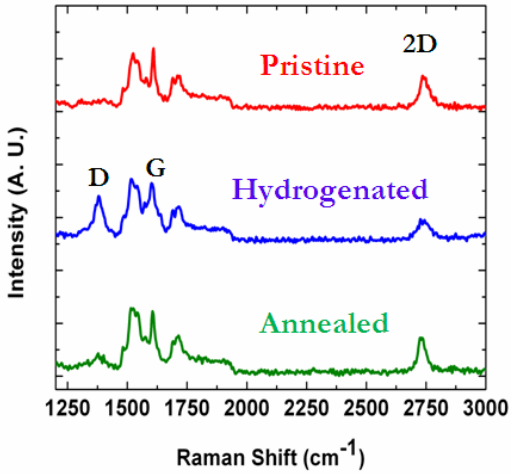

Figure 4.5. The Raman spectra of EG as-fabricated (red), after hydrogenation (blue), and after thermal annealing (green). The hydrogenation process induces the D-peak, and the thermal anneal serves to decrease the disorder-induced D-peak significantly.

4.2 HYDROGENATION OF EXFOLIATED GRAPHENE NANORIBBONS

The development of the HSQ trimming and hydrogenation processes was followed by electrical measurements of the back-gated exfoliated GNR devices. After the trimming and hydrogenation of the exfoliated GNRs, the samples were loaded into a Lake Shore Cryotronics cryogenic probe station and pumped down to a pressure of $P = 10^{-6}$ Torr to remove any atmospheric adsorbates. The electrical measurements were performed with a Keithley 2612 source meter in the two-point mode at room temperature.

In order to determine the change in the electrical transport as a result of the HSQ trimming process, exfoliated GNR devices were tested before and after the exposure to the 0.1% dilution of HF (Figure 4.6). The ExG was found to be relatively charge-neutral (V_{Gmin} ~ -5 V) as expected due to the careful substrate preparation performed before the exfoliation of the graphene flakes. The trimming of ~ 5 nm of HSQ laterally from the exfoliated GNRs resulted in a minimal shift of V_{Gmin} to 0 V. The cause of this shift may be due to slight atmospheric doping of the exposed graphene region during processing; water vapor or oxygen from the atmosphere leads to p-type doping of the graphene [76].

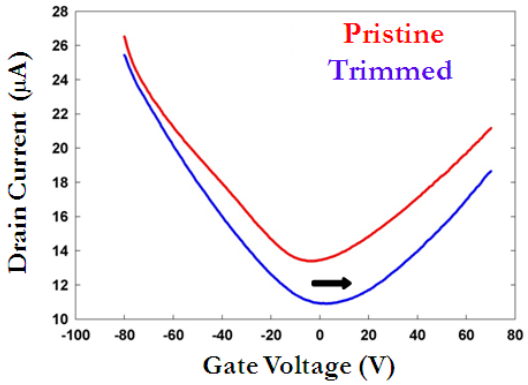

Figure 4.6. The *I-V* curve for a 30-nm exfoliated GNR subjected to HSQ trimming to expose the GNR edges. The removal of ~ 5 nm of HSQ laterally caused a positive shift in the location of V_{Gmin} from -5 V to 0 V, possibly as a result of slight atmospheric doping.

In contrast to the p-type doping induced during the trimming process, the electrical transport data for the hydrogenated exfoliated GNRs revealed a significant n-type shift of V_{Gmin} to ~ -18 V (Figure 4.7). The negative shift of V_{Gmin} may be attributed to two separate mechanisms: hydrogen attachment and plasma exposure. Hydrogen generally acts as an n-type dopant for graphene, so the attachment of the hydrogen atoms to the GNR edge may manifest as slight n-type doping of the entire GNR. In addition, the exposure of the HSQ thin film to plasma, as experienced during the hydrogenation step, can cross-link the HSQ and lead to doping. The previous work [68] suggests that n-type doping is induced in HSQ-coated ExG upon brief exposure to plasma. Although the exfoliated GNRs used in the hydrogenation study were exposed to the plasma for at least 2 min., the presence of the shield structure may have slowed the rate of the HSQ cross-linking and allowed for slight n-type doping of the graphene.

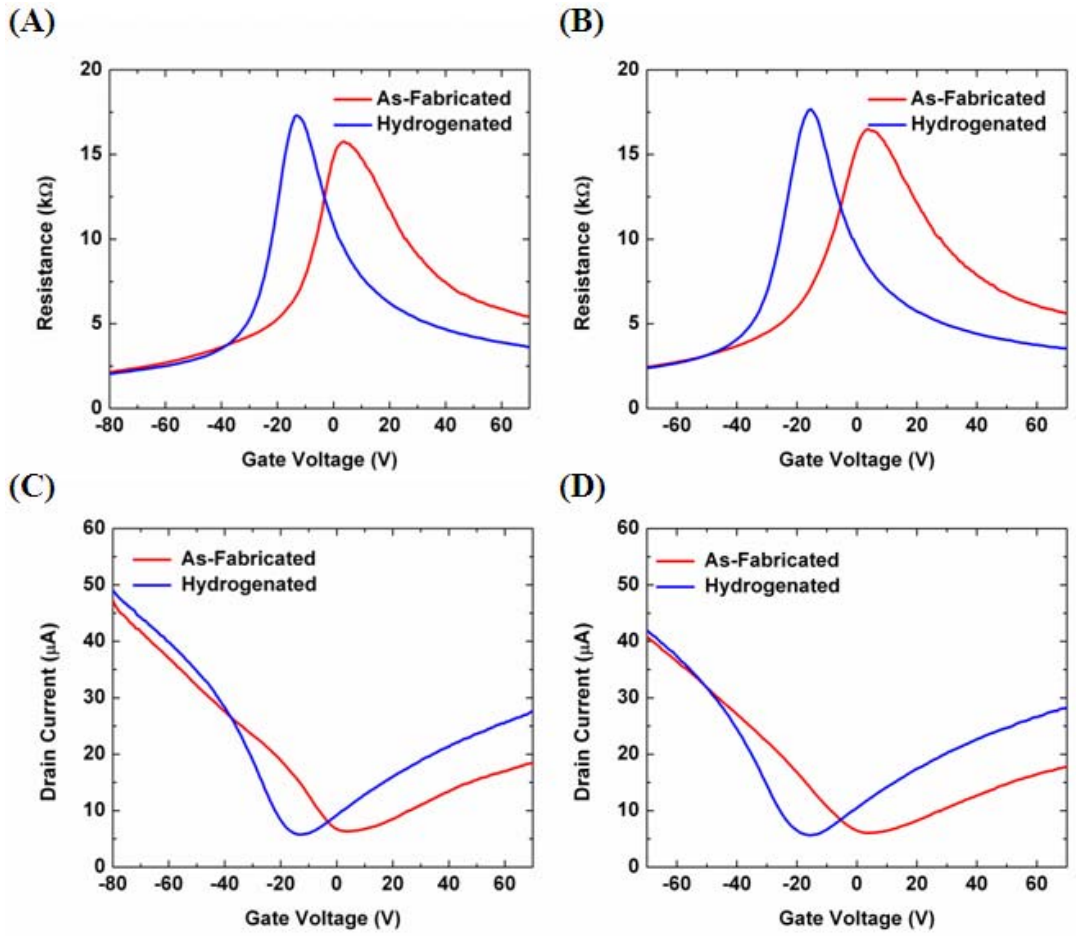

Figure 4.7. The electrical measurements of a 30-nm exfoliated GNR are shown for two representative devices before and after the hydrogenation of the GNR edges. (A-B) The resistance vs. gate voltage is plotted for the two devices. A negative shift of V_{Gmin} occurs, as well as a slight increase in the maximum resistance, after the edge hydrogenation. (C-D) The drain current vs. gate voltage is plotted for the two devices. The minimum drain current is slightly reduced and the symmetry of the curves improves after the edge hydrogenation.

In order to determine any improvement in the electrical transport as a result of the hydrogenation process, the mobility of the GNRs was extracted using the method outlined in Chapter 3.3. The conductivity was evaluated at two set carrier densities of n = 5 x 10^{12} cm^{-2} and n = 7 x 10^{12} cm^{-2}, and the gate capacitance was calculated to be c_G = 7.14 x 10^{-8} F/cm^2. Fringe-field effects for the 30-nm exfoliated GNR were also taken into account by utilizing COMSOL simulations. The as-fabricated exfoliated GNRs exhibited

an average mobility of μ = 158 $cm^{2/}$V-s, and the mobility increased slightly to μ = 162 $cm^{2/}$V-s after the hydrogenation process (Table 9). In addition, the modulation of the exfoliated GNRs showed slight improvements from $I_{on}/I_{off} \sim 7.5$ to $I_{on}/I_{off} \sim 8.5$.

Table 9. The characteristic properties of 30-nm exfoliated GNRs before and after hydrogenation.

	V_{Gmin} (V)	I_{on}/I_{off}	n (cm^{-2})	μ (cm^2/V-s)	n (cm^{-2})	μ (cm^2/V-s)
Device 1						
As-Fabricated	3.9	7.5	5 x 10^{12}	222	7 x 10^{12}	159
Hydrogenated	-13.4	8.5	5 x 10^{12}	231	7 x 10^{12}	165
Device 2						
As-Fabricated	3.4	7.7	5 x 10^{12}	218	7 x 10^{12}	156
Hydrogenated	-15.3	8.4	5 x 10^{12}	223	7 x 10^{12}	159

Upon comparison to the data collected from all the exfoliated GNR devices subjected to hydrogenation, a small number (< 10%) of the tested devices showed a decrease in both the mobility and the modulation. Further analysis revealed that the devices which exhibited degradation of the electrical transport properties were located on the outer regions of the larger SiO_2/Si substrates. Due to the location of these devices, the hydrogen plasma used to hydrogenate the GNR edges may have inadvertently etched the exposed graphene, as these regions of the sample were in the direct vicinity of the openings in the shield structure. The result of this type of etching would be a narrower GNR that was expected to display a reduced mobility due to the smaller width and the presence of the LER induced during processing.

The experiments based on the hydrogenation of exfoliated GNRs revealed only minimal improvements in the electrical transport properties. The careful development of the trimming and hydrogenation process, as characterized by Raman spectroscopy,

suggested a robust and effective process for hydrogen attachment, but the transfer of these processes to the tested devices did not result in significant improvements in the GNR electrical behavior. An explanation for the lack of positive results may have been inadvertent atmospheric doping of the exposed GNR edges between the HSQ trimming step and the hydrogenation process. The samples were only exposed to the atmosphere for a brief period of time between the two processes, but the large reactivity of the exposed graphene edges may have allowed for atmospheric adsorbates to attach to the graphene. This explanation was further supported by the slight positive shift of V_{Gmin} after the trimming step (Figure 4.6). The subsequent hydrogenation process would then be only minimally effective, as the majority of the broken C bonds at the GNR edges would have already been saturated. Furthermore, the hydrogenation of the extreme edges of the GNR may not be sufficient to induce any significant changes in the electrical transport properties. If hydrogen atoms were only able to attach to the broken C bonds at the GNR edge and not to the exposed basal plane of the graphene, only a minimal change in the electrical behavior would be expected.

4.3 HYDROGENATION OF EPITAXIAL GRAPHENE NANORIBBONS

The results of the hydrogenation of exfoliated GNRs showed only minimal improvements in the conductivity at narrow line widths, but the process was transferred to the EG platform to determine the efficacy of the edge hydrogenation to GNRs on a different substrate. Previous experiments based on ExG have revealed a strong affinity for the material to become p-doped upon exposure to the atmosphere [77]. In contrast, EG appears to be much less susceptible to atmospheric doping, as evidenced by the

repeatable electrical measurements made on AG epitaxial samples after long periods of exposure to the ambient environment. As discussed in the previous section, a possible reason for the lack of significant changes in the electrical behavior of the exfoliated GNRs could be inadvertent atmospheric doping which decreases the efficacy of the hydrogenation process. In this section, the efficacy of the hydrogenation process on epitaxial GNRs is presented and compared to the results of the previous section.

As described in the first part of this chapter, the EG platform is more difficult to use as an accurate probe for the efficacy of hydrogenation because of the top-gate device design. Before gated measurements of the epitaxial GNRs can be made, all steps of the process (i.e., trimming, hydrogenation, top-gate fabrication) must be completed. This leads to the necessity to compare and contrast the electrical behavior of individual EG samples, as opposed to testing identical devices after each processing step as presented in Chapter 4.2. To minimize significant changes between the EG samples which may skew the data, a batch of EG samples was selected that exhibited similar AG sheet resistance, charge carrier density, and substrate morphology as determined by AFM imaging. Similarly, the EG samples were processed side by side with identical fabrication techniques to further eradicate variation in the hydrogenation data.

Before hydrogenation was performed on the epitaxial GNRs, the four-point resistance of the GNR devices was measured before and after the HSQ trimming process to determine any appreciable changes in the resistance. A trimming process of 10 sec. in a 0.1% dilution of HF was used to remove ~ 5 nm of the HSQ laterally from the GNRs. As witnessed for the exfoliated GNRs in Chapter 4.2 (Figure 4.6), the average device resistance decreased by ~10% after the HSQ trimming. After the trimming process, the

EG samples were exposed to an identical hydrogenation process to that of exfoliated GNRs, and the top-gate structure was subsequently fabricated according to the process outlined in Chapter 3.1. A comparison between identically-sized GNRs on an AG sample and a hydrogenated sample are shown in Figure 4.8 for two separate GNR line widths. The location of V_{Gmin} was found to shift slightly in the negative direction after the edge hydrogenation, similar to the behavior witnessed for exfoliated GNRs.

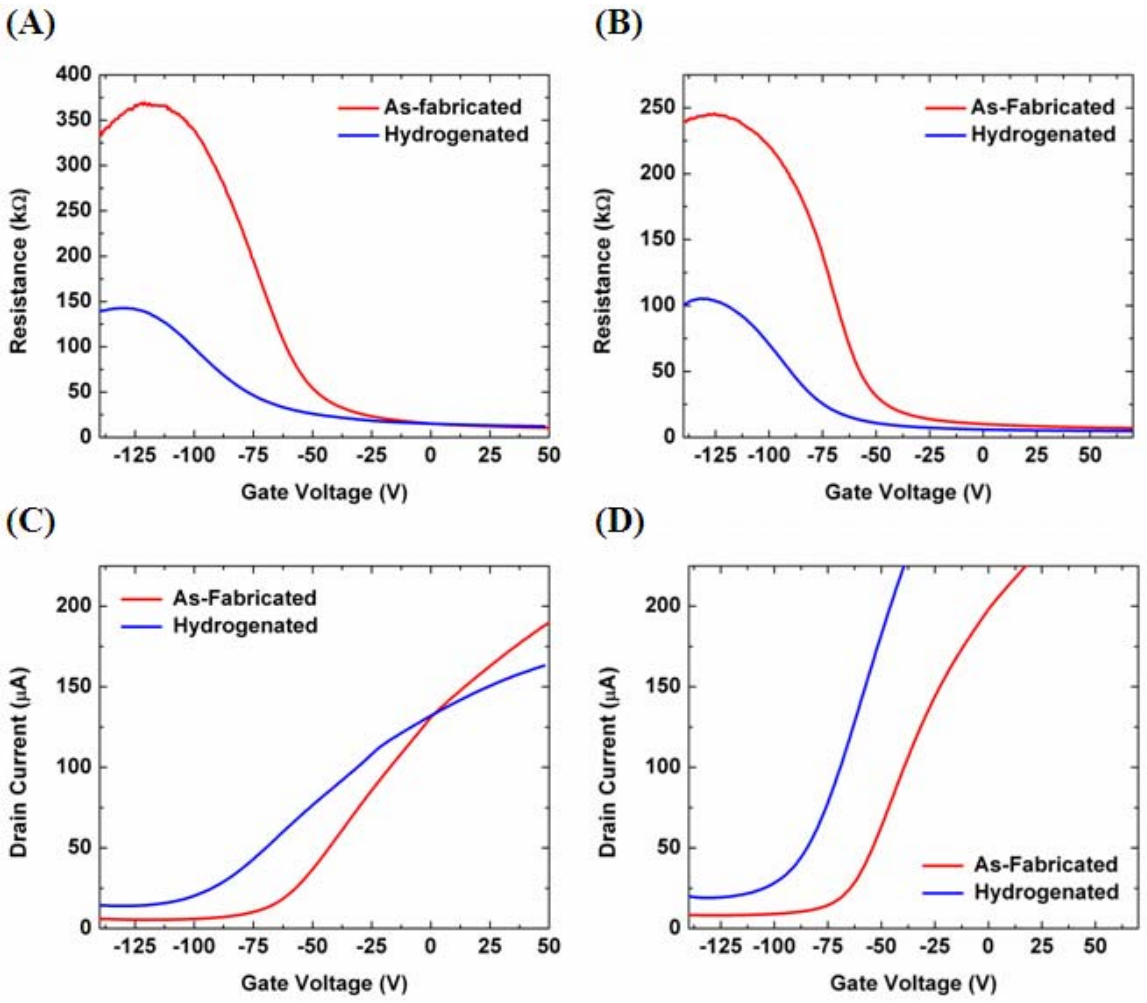

Figure 4.8. The electrical measurements of a 60-nm (A, C) and a 100-nm (B, D) GNR device are shown for the as-fabricated (red) and hydrogenated (blue) EG samples. (A-B) The resistance vs. gate voltage is plotted for the two devices. A negative shift of V_{Gmin} occurs, as well as a significant decrease in the maximum resistance, after the edge hydrogenation. (C-D) The drain current vs. gate voltage is plotted for the two devices. The minimum drain current is slightly increased after hydrogenation.

In contrast to the exfoliated GNRs, the mobility of the epitaxial GNRs (Table 10) was significantly improved upon hydrogenation of the GNR edges. When considering the mobility of the devices at a carrier density identical to that used for the exfoliated GNR analysis, the mobility was seen to increase by 35-50% for the hydrogenated epitaxial GNRs. Although the mobility of the devices was seen to improve, the modulation was reduced for both devices. In comparison to the values obtained for even narrower exfoliated GNR devices (W = 30 nm), the modulation values of the epitaxial GNRs, even after hydrogenation, was significantly larger, suggesting improved switching efficacy over that afforded by ExG devices. The improved results of the epitaxial GNR behavior after hydrogenation appear to confirm the assumption made in regard to atmospheric doping of the ExG. The exposed edges of the exfoliated GNRs may not be efficiently hydrogenated due to atmospheric adsorbates saturating the dangling bonds at the GNR edge, and therefore only minimal changes in the electrical behavior due to hydrogenation would be witnessed for the ExG. Because the EG used in this work was less susceptible to atmospheric doping, the hydrogenation process appears to be effective in improving the carrier mobility of the GNRs.

Table 10. The characteristic properties of 60-nm and 100-nm epitaxial GNRs as-fabricated and after the hydrogenation process.

	V_{Gmin} (V)	I_{on}/I_{off}	n (cm^{-2})	μ (cm^2/V-s)	n (cm^{-2})	μ (cm^2/V-s)
Device 1						
As-Fabricated	-122	38	5×10^{12}	429	7×10^{12}	307
Hydrogenated	-128.5	12	5×10^{12}	581	7×10^{12}	416
Device 2						
As-Fabricated	-126	35	5×10^{12}	355	7×10^{12}	254
Hydrogenated	-131.5	22	5×10^{12}	545	7×10^{12}	389

To further understand the implications of the edge hydrogenation of epitaxial GNRs, devices of varying line width (20 nm ≤ W ≤ 1 μm) were fabricated on multiple samples to estimate the size-dependent conductivity. The resistance values of the GNR devices were obtained in the four-point mode at a gate voltage of 0 V; this type of measurement was performed to allow for an accurate comparison to the original size effect work presented in Chapter 3.3. The data collected for four individual EG samples is presented in Figure 4.9.

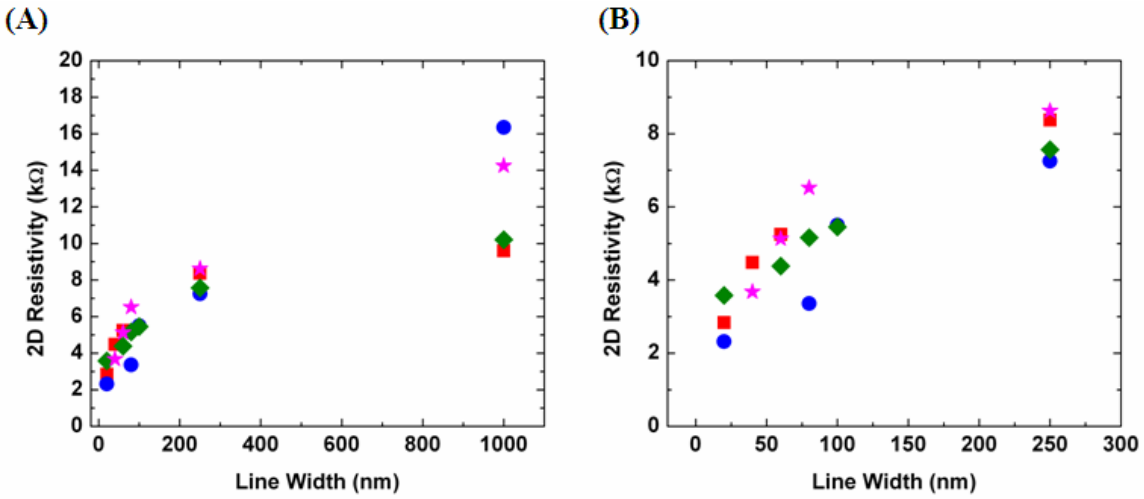

Figure 4.9. The 2D resistivity vs. line width for four individual EG samples (different colors/symbols) subjected to hydrogenation of the GNR edges. (A) The full range of GNR widths (20 nm ≤ W ≤ 1 μm) is shown. (B) A smaller range of GNR widths (20 nm ≤ W ≤ 250 nm) is shown for clarity.

In contrast to the expected size effect behavior first presented in Chapter 3.3, the GNR devices subjected to the hydrogenation process display an inverse size-dependent conductivity relationship. The largest GNR devices show the most resistive behavior; a 1-μm GNR exhibits an average 2D resistivity of ρ_{2D} = 12.6 kΩ and a 250-nm GNR exhibits an average 2D resistivity of ρ_{2D} = 8 kΩ. When considering the narrow GNR widths, the

resistivity decreases greatly; a 20-nm GNR displays an average resistivity of ρ_{2D} = 3 kΩ. To further elucidate the disparity between the samples used in the original size-dependent conductivity study and the samples exposed to the edge hydrogenation process, the extreme results from Chapter 3.3 (Figure 3.6) are plotted against the hydrogenation samples in Figure 4.10.

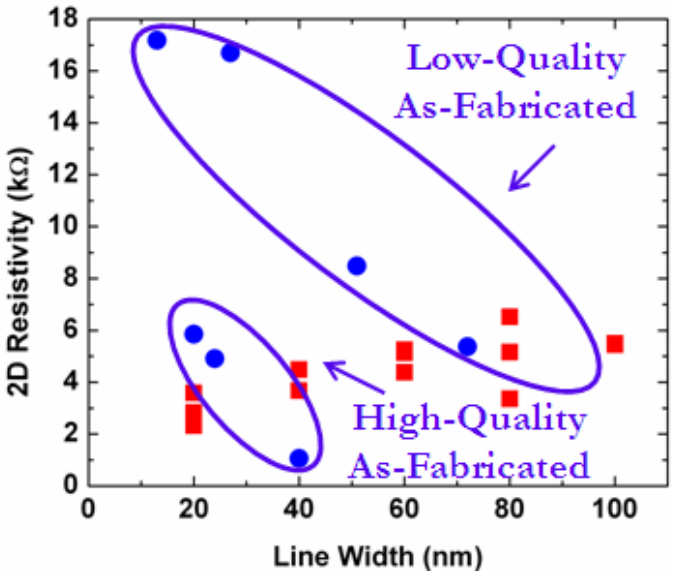

Figure 4.10. The 2D resistivity vs. line width for as-fabricated epitaxial GNRs (blue) is compared to hydrogenated epitaxial GNRs (red). The best (high-quality) and worst (low-quality) size effect data for the as-fabricated epitaxial GNRs is circled in blue for clarity.

To understand the disparity in the size-dependent conductivity between the as-fabricated samples and those samples subjected to the hydrogenation process, a careful analysis of the scattering sources first presented in Chapter 3.3 was performed. Upon hydrogenation of the GNR edges, the LER was expected to be reduced as a result of the conversion of the exposed graphene at the GNR edge into a semi-insulating state. With the reduction or eradication of the LER scattering in the GNRs, the size-dependent

conductivity was then expected to be only a function of boundary scattering due to terrace step edges, grain boundaries, and regions of varying graphene thickness.

For the batch of samples subjected to the hydrogenation process, AFM imaging (Figure 4.11) revealed an average terrace width of $W_T \sim 5$ μm, and the terrace angle with respect to the sample edge was found to be ~ 90° for all of the samples. The GNR devices patterned on the samples were designed with a length of $L = 2$ μm, so even without careful alignment of the GNR devices to the substrate terraces, most GNR devices should have been contained on a single terrace. As with all the samples presented in this work, SEM imaging was performed after the GNR patterning to determine which devices were found to cross a step edge. Those devices crossing a step edge were not electrically tested in order to obtain an accurate comparison across the individual GNR devices.

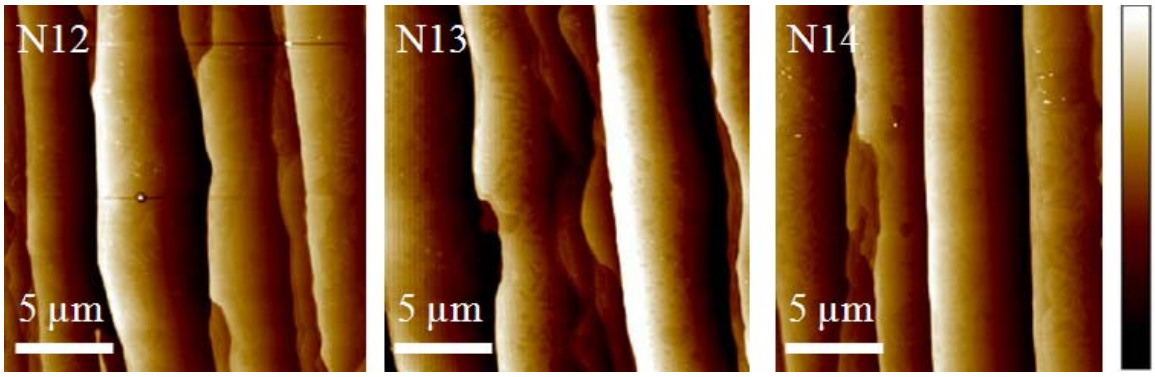

Figure 4.11. AFM images of the AG epitaxial samples used for the hydrogenation process. The samples are characterized by large terraces (average $W_T \sim 5$ μm) and a nearly perpendicular terrace angle with respect to the sample edge. The gradient scale bar corresponds to a 15-nm height variation.

Although the substrate morphology of the hydrogenated samples was found to be optimal for GNR fabrication, boundary scattering within a terrace was still expected as a result of grain boundaries and possible graphene thickness variations. When considering

the size-dependent conductivity behavior (Figure 4.9), the larger resistivity for larger GNR line widths can be understood in the context of the boundary scattering. For a narrow GNR ($W \leq 100$ nm, $L = 2$ μm) without the influence of LER scattering, removed during the hydrogenation process, the boundary scattering was expected to be minimal because of the small size of the patterned area. As the GNR width was increased, the probability of charge carriers within the GNR encountering a grain boundary or a thickness variation increased significantly. This is shown pictorially in Figure 4.12 for clarity; the GNRs were arbitrarily sketched on a small region of a larger sample to further elucidate the sources of boundary scattering. The GNR widths are not drawn to scale. For a 20-nm GNR, the surface of the graphene exposed to the GNR patterning is observed to be smooth, suggesting uniform graphene thickness. In contrast, the larger, 100-nm GNR is obviously patterned over a region of graphene that experiences thickness variations, as witnessed by the color gradation in the AFM image. When considering the increased probability of charge carriers encountering boundary scattering in larger GNRs, the resistivities of the wide GNRs was predictably larger than that of the narrow GNRs.

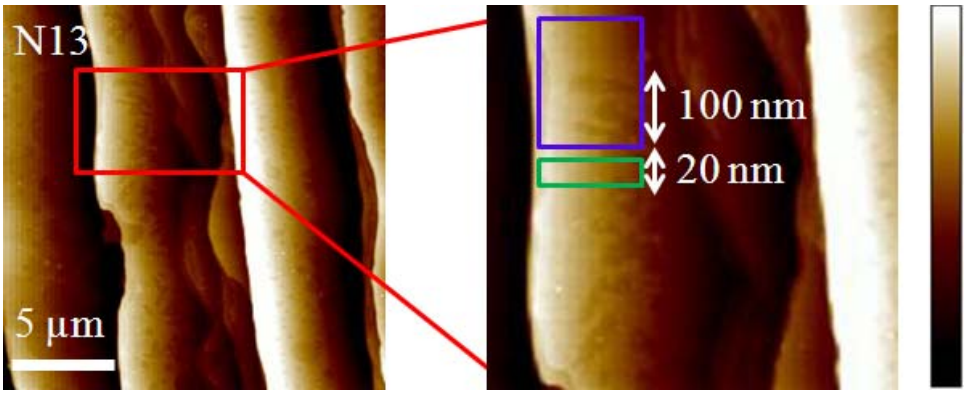

Figure 4.12. AFM images highlighting a particular region of a larger EG sample used in the edge hydrogenation study (shown on the right). Two representative GNRs ($L = 2$ μm) of width $W = 20$ nm (green) and $W = 100$ nm (blue) are shown on the zoomed region. Careful analysis of the graphene regions where each GNR is patterned show increased thickness variation and possible grain boundaries for larger GNRs.

The selective hydrogenation of the edges of both exfoliated and epitaxial GNRs was systematically investigated and found to induce significant changes in the electrical transport properties and the size-dependent conductivity. The trimming of the HSQ resist atop the fabricated GNRs was optimized using a dilution of HF, and the subsequent process of hydrogenating the exposed graphene regions was accomplished with the use of a custom-designed shield structure and a low-power hydrogen plasma. The optimization of both the HSQ trimming and the hydrogenation processes was performed on large-area ExG and EG samples; the successful hydrogenation was confirmed via Raman spectroscopy. For exfoliated GNRs, the edge hydrogenation was found to induce minimal changes in the electrical transport properties, which can be understood in the context of inadvertent atmospheric doping that reduces the efficacy of the hydrogenation process. In contrast, epitaxial GNRs subjected to edge hydrogenation showed improved carrier mobility, and significantly larger modulation values in comparison to those obtained both before and after the hydrogenation of exfoliated GNRs. In addition, the edge hydrogenation was extremely successful at mitigating the lithographically-patterned LER and improving the detrimental size-dependent conductivity originally investigated in Chapter 3.3. Specifically, the size effect behavior was found to invert upon hydrogenation of the epitaxial GNR edges. The narrowest GNRs experienced the lowest 2D resistivity values, and larger-area EG was found to be less conductive. This behavior was explained in the context of increased boundary scattering for larger GNR line widths; the probability of charge carriers encountering a grain boundary or graphene thickness variation increased as a function of the increasing width.

In conclusion, the hydrogenation of epitaxial GNR edges was shown to be highly effective at minimizing the LER scattering, and improving the overall conductivity as the GNR line widths were scaled down. This work represents a significant, positive push towards utilizing nanoscale EG in transistor devices, as high charge carrier mobility and large modulation values were found to be achievable with epitaxial GNRs exposed to edge hydrogenation.

CHAPTER V –DOPING OF EPITAXIAL GRAPHENE NANORIBBONS

For graphene to function in a complementary manner, parallel to complementary metal-oxide-semiconductor (CMOS) devices, the ability to fabricate n- and p-type regions is required. The realization of a number of promising device architectures in graphene relies on the formation of p-n junctions [25, 27], thereby furthering the need for a reliable complementary doping technique. If graphene is to become integrated with silicon, complementary doping is required to avoid the unintentional formation of p-n junctions at the interfaces between the two materials. In addition, the possibility of a monolithic system based on EG, where the transistor and the interconnect material are seamlessly integrated, would require tunable doping to allow for the optimization of the current-carrying capacity in various conducting regions.

Presently, the major barrier to creating p-type regions in EG is the presence of the nonconducting buffer layer, as described further in this chapter, which causes the heavy n-type doping of the first graphene monolayer and shifts the Fermi level ~ 0.4 eV above the Dirac point [78] (Figure 5.1). The objective of this study was to investigate how to counteract or reduce the strong, intrinsic, n-type doping of EG on SiC (0001), and thereby provide a route towards complementary doping.

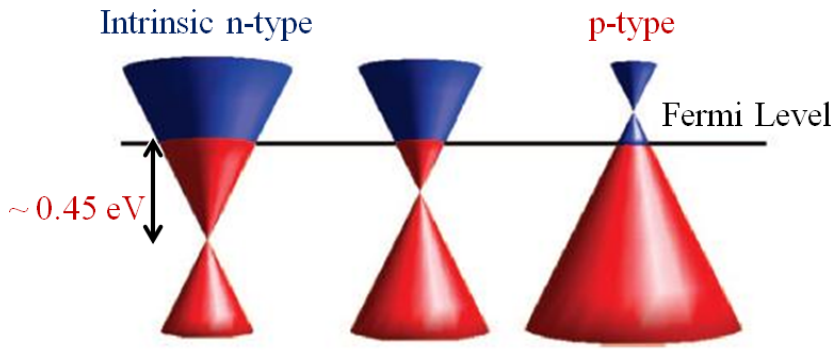

Figure 5.1. The Dirac cone of doped EG. The Fermi level of intrinsic, n-type graphene is pinned in the conduction band ~ 0.45 eV above the Dirac point. P-type EG on SiC (0001) would require a negative shift of the Fermi level of more than 0.45 eV.

A variety of methods have been employed to counteract the n-doping of EG, with most of the experimental evidence being obtained on large-area graphene via spectroscopic studies that provide limited insight into the electrical transport properties. The intercalation of H atoms has been shown to saturate the dangling bonds from the Si atoms in the SiC substrate, effectively creating a freestanding graphene monolayer [79] that exhibits charge neutrality after annealing. Similarly, Au atoms have been used in an intercalation process [80] to shift the Fermi level closer to the Dirac point in EG. Weak hole injection into EG has also been accomplished through the surface adsorption of gas molecules [81] such as NO_2. In addition, the noncovalent functionalization of EG accomplished by using aromatic molecules has succeeded in shifting the Fermi level to the Dirac point [82]. The controllable and tunable p-type doping of epitaxial GNRs resulting in a shift of the Fermi level below the Dirac point has not yet been achieved in these studies [79-82]. In this chapter, two separate techniques were used to shift the location of the Fermi level of epitaxial GNRs below the Dirac point and thereby achieve p-type EG. The first technique was based on the thermal annealing of the negative-tone e-

beam resist HSQ; a process of this kind would allow for selective doping of specific graphene regions. The second technique provides a blanket doping of the entire EG sample through the intercalation of hydrogen atoms underneath the graphene film. This chapter serves as a systematic investigation of how these two doping techniques affect the electrical transport in epitaxial GNRs.

5.1 CHEMICAL DOPING VIA THERMAL ANNEALING OF HSQ

The fabrication of GNRs is generally accomplished with the use of negative-tone e-beam resists and e-beam lithography, although novel techniques [32, 37] have recently been successful in the patterning of GNRs without the need for lithography or etching. When using the e-beam resist HSQ to pattern GNRs, the resist is often left intact during the electrical testing of the fabricated devices due to the difficulties encountered when attempting to fully remove the HSQ after the resist development and plasma processing. The structure of HSQ is similar to that of SiO_2, and therefore the resist can be partially removed with exposure to a wet etch in HF. Unfortunately, the wet etch is not capable of removing all of the HSQ, and residue is often left behind; the result is a nonuniform coating of resist which can skew the data obtained from the electrical measurements of the GNRs. In order to avoid this issue, the HSQ was left atop the GNRs during the electrical testing in this work to provide for an accurate comparison of the data across the individual devices. In addition, the thin film (~ 30-nm thick) of HSQ adds to the overall gate-oxide stack and thereby allows for increased gate voltage sweeps without premature breakdown of the gate during the electrical testing. Furthermore, the HSQ thin film can also act as a seed layer for ALD of the top-gate oxide [36], so it appears advantageous to

leave the resist intact for processing benefits. For these reasons, it was beneficial to understand how to utilize the HSQ resist as a dopant source for the GNRs. Furthermore, the development of a methodology to selectively dope EG regions, as opposed to large-area graphene, is extremely important for digital logic applications because the doped EG can be used to build complementary devices, induce a transport gap, and explore many novel device concepts based on p-n junctions.

5.1.1 HSQ Doping of Exfoliated Graphene

After the spin-coating of the negative-tone resist HSQ, the material appears as a cagelike structure made up of hydrogen, silicon, and oxygen (Figure 5.2 A). The structure of the film can then be altered by the application of energy in the form of e-beam irradiation, plasma exposure, or thermal annealing. The bonds between Si and H are easily broken during such processes [83], resulting in the formation of molecular H_2 that leaves the film via out gassing. The remaining film is then O-rich, and breaks down into a networklike structure [84] with reduced porosity and increased density (Figure 5.2 B).

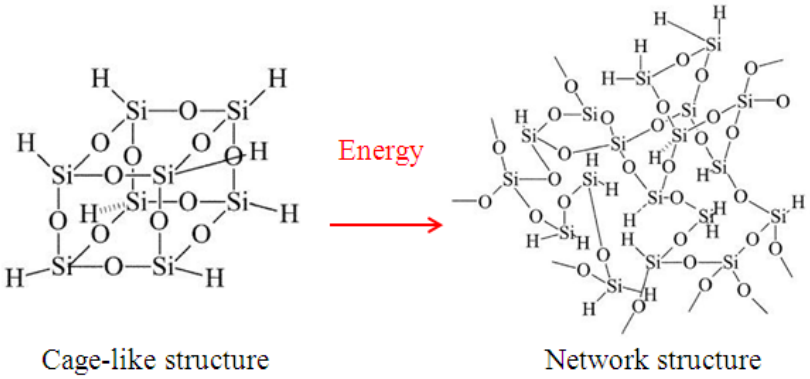

Figure 5.2. The structure of HSQ. (A) The cagelike structure of HSQ after spin-coating. (B) The networklike structure of HSQ after the application of energy.

Previous experimental work based on a study of various energy sources applied to HSQ atop ExG revealed the impact of this doping technique on the electrical transport properties of the graphene [68]. Exfoliated graphene was an excellent platform for such a study, as the material can be obtained in a relatively charge-neutral form through careful processing techniques. By tailoring the e-beam dosage of the HSQ film, the ExG was found to be tunable from heavy n-type doping to strong p-type doping. After the spin-coating and post-baking of the HSQ, the charge-neutral ExG was found to become n-type. Upon subsequent e-beam irradiation of the HSQ resist, the ExG was found to become heavily p-type (Figure 5.3). In general, low dosages of e-beam irradiation resulted in the n-type doping of charge-neutral ExG, while higher dosages (> 1500 $\mu C/cm^2$) yielded p-type doping of the ExG. Furthermore, the ExG samples were exposed to an Ar plasma for various amounts of time to determine how the plasma, commonly used to etch excess graphene, would affect the HSQ doping of the graphene. For short exposure times, the HSQ-coated graphene exhibited n-type doping; for longer exposure times, further cross-linking of the HSQ occurred and caused p-type doping.

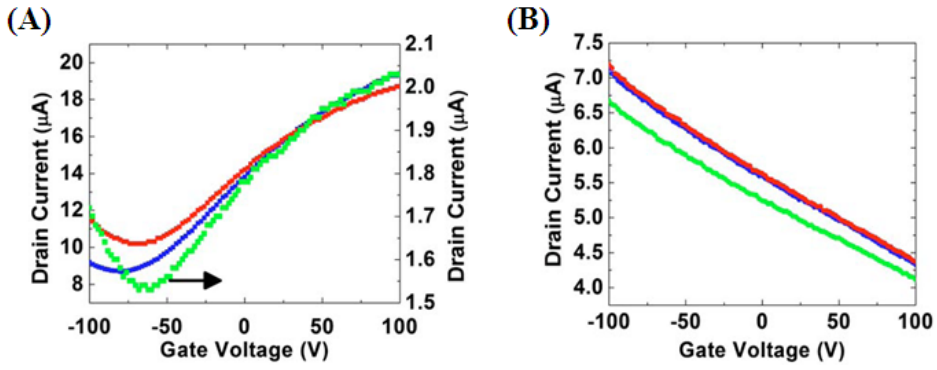

Figure 5.3. The *I-V* curves for ExG exposed to varying e-beam dosages [68]. The colored curves correspond to three identical devices. (A) N-type ExG after spin-coating and baking of the HSQ resist. (B) P-type ExG after e-beam irradiation of the HSQ resist.

In contrast, a study of the HSQ doping effects on EG was expected to yield disparate results, as the EG produced on SiC (0001) does not display charge neutrality after growth. The heavy n-type doping of the EG makes the realization of p-type doping more challenging. In addition, the ExG study made use of large-area graphene regions as opposed to GNRs. When fabricating GNRs of varying width, specific e-beam dosages are necessary to fully expose the pattern and allow for proper development, as outlined in Chapter 3.1.3. This processing requirement does not allow for the excessive changes in the e-beam dosage necessary to dope the graphene either n-type or p-type as shown in the ExG study. In order to use the HSQ resist as a dopant source for epitaxial GNRs, a thermal annealing method was realized to supplement the variation of the e-beam dosage.

5.1.2 HSQ Doping of Epitaxial Graphene Nanoribbons

The thermal annealing of HSQ was used in this work to modify the density of the cross-linked HSQ thin films atop the epitaxial GNRs, thereby resulting in further enhancements of the graphene basal plane p-type doping. The annealing temperature was kept in a range ($T \sim 250$ °C) where only a structural change in the film was expected [85], resulting in an increase of the film density and a decrease of the film porosity. The increased density of the O-rich film allowed more O atoms to contact the graphene surface, allowing for charge transfer to occur between the graphene and the oxygen, and thereby resulting in the p-type doping of the epitaxial GNRs. The modification of the density of the HSQ film was the key to producing sufficient graphene basal plane doping that was capable of overcoming the n-type doping from the SiC substrate. Other

techniques that rely on molecule adsorption or the use of less dense film coatings fail to provide enough dopants, and are thus incapable of producing p-type epitaxial GNRs.

Epitaxial GNR top-gated transistors were fabricated with the process outlined in Chapter 3.1 for this study. This structure was used to obtain electrical measurements that would allow for the determination of V_{Dirac} and the measurement of the minimum conductivity point (V_{Gmin}) shift as a function of the chemical doping. The samples used for the top-gate transistor devices were found to have an average charge carrier density of $n \sim 10^{13}$ cm^{-2} and an average mobility of μ = 2500 cm^2/V-s directly after growth, as determined from four-point electrical testing in the van der Pauw and Hall configurations. The epitaxial GNRs used for this study were 20 nm in width and 2 μm in length.

After the device fabrication, the samples were loaded into a Lake Shore Cryotronics cryogenic probe station, and the chamber was pumped down to a pressure of $P = 10^{-6}$ Torr to remove any atmospheric adsorbates that could affect the doping levels of the graphene. The electrical measurements were performed with a Keithley 2612 source meter in the four-point mode to eliminate the contact resistance element. Before the measurements were taken, the probe station was cooled down to a temperature of 77 K with liquid nitrogen; this was necessary to improve the quality of the dielectric and allow for a large enough gate voltage sweep so that the Dirac point was visible. During the electrical testing, the gate leakage current was carefully monitored and kept below 10 nA to ensure the accurate measurement of the top-gate transistors and to avoid the premature breakdown of the gate. In addition, a pulsed-gate bias technique was used to minimize the hysteresis during the dual sweep of the gate voltage, thereby allowing for the precise extraction of the doping level [86].

The as-fabricated devices showed a negative minimum conductivity point of V_{Gmin} = -54 V, corresponding to an n-type carrier density of ~ 1.1 x 10^{13} cm^{-2} (Figure 5.4). After the initial electrical testing, the samples were annealed on a hotplate in the ambient environment at 250 °C for 24, 48, and 72 hours; the samples were then loaded back into the cryogenic probe station and the system was pumped down overnight before the electrical testing was performed again. After 72 hours of annealing, V_{Gmin} for the three devices tested had shifted by more than +50 V to positive gate voltages (V_{Gmin} = +3 V), indicating a p-type carrier density of ~ 6.5 x 10^{11} cm^{-2} in the GNRs (Figure 5.4). Extended annealing beyond 72 hours did not result in any further shifts of V_{Gmin} or changes to the *I-V* curves, suggesting that all of the available dangling O bonds in the HSQ thin film had been allowed to bind with the graphene surface. In addition, the repeated electrical testing after the samples were removed from vacuum and left in the ambient environment for two weeks showed no significant changes to the *I-V* curves, suggesting that the HSQ doping method presented herein is stable.

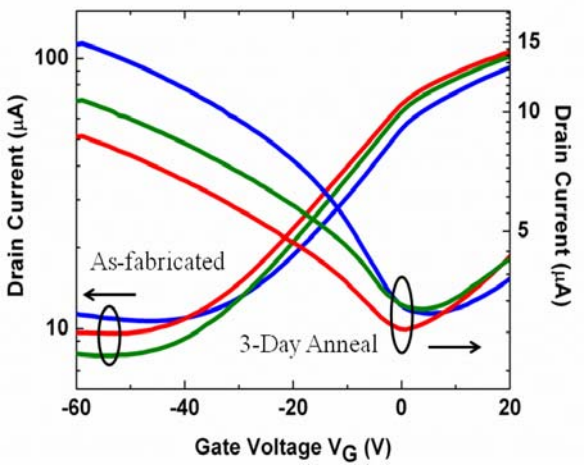

Figure 5.4. The *I-V* curves for the top-gated EG transistors before and after the HSQ annealing. The colored curves correspond to three identical devices. A shift in the minimum conductivity point of more than +50 V is observed, indicating the formation of p-type epitaxial GNRs.

In order to determine any improvement in the electrical transport as a result of the thermal annealing of the HSQ, the mobility of the GNRs was extracted using the method outlined in Chapter 3.3. The conductivity was evaluated at a set carrier density of n = 9.9 x 10^{12} cm^{-2}, and the gate capacitance was calculated to be c_G = 2.66 x 10^{-8} F/cm^2. Fringe-field effects for the 20-nm epitaxial GNRs were also taken into account by utilizing COMSOL simulations. For the GNRs in this study, the testing of the as-fabricated devices yielded a mobility of μ = 240 cm^2/V-s. This was a significant reduction of the mobility from the AG average 2D mobility of μ = 2500 cm^2/V-s obtained from the Hall effect testing. The mobility degradation from the AG value was due mostly to the size effect [69] caused by the lithographically-patterned LER as described in Chapter III. The size effect work predicted a mobility range of 100-500 cm^2/V-s for a GNR width of 20 nm fabricated with this process, so the fabricated epitaxial GNRs used in this study fitted well within the expected range of values.

After annealing of the HSQ for 72 hours, the mobility was seen to further reduce to μ = 70 cm^2/V-s. For charged impurity scattering in graphene, the mobility, the minimum conductivity, and the on/off current ratio are all expected to reduce as a function of the doping [87]. The samples tested in this work show a mobility reduction of 70%, a minimum conductivity decrease of 60-80%, and a change in I_{on}/I_{off} from 8 to 3.5 after 72 hours of HSQ annealing. The charged impurity scattering in the studied samples was directly attributed to the increased number of dopants in contact with the basal plane of the graphene as the density of the HSQ film increased. Since the basal plane of the GNRs was passivated by the HSQ film and the top-gate dielectric, only negligible p-type doping or changes in the mobility as a result of any atmospheric adsorbates was expected.

To determine the Fermi energy corresponding to the location of the minimum conductivity point, the relation [33]:

$$E_F(n) = sgn(n)\hbar v_F\sqrt{\pi|n|} \quad (5.1)$$

was used, where n was the charge carrier density evaluated at V_{Gmin}, E_F was the Fermi energy, $\hbar$ was Planck's constant divided by 2π, and v_F was the Fermi velocity. The Fermi level shift as a function of the annealing time is shown in Figure 5.5. As the annealing time was increased, the Fermi level moved closer to the Dirac point and then eventually became negative, indicating the p-type doping of the epitaxial GNRs.

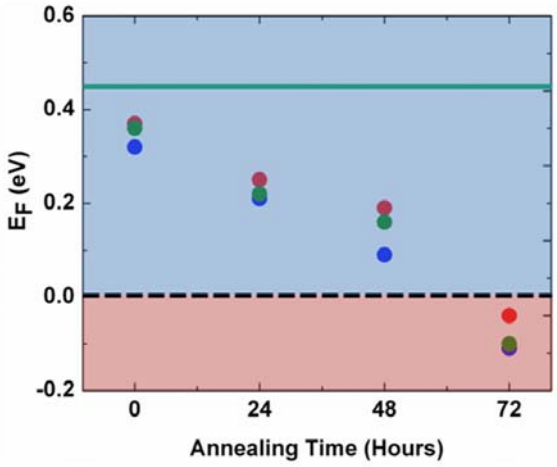

Figure 5.5. The Fermi level is plotted as a function of the HSQ annealing time. The colored symbols correspond to three identical devices. For a 72-hour anneal, p-type epitaxial GNRs were observed, with the Fermi level location ~ 0.1 eV below the Dirac point. The green band represents the intrinsic Fermi level (~ 0.45 eV) for EG on SiC (0001). The black dashed line corresponds to the Dirac point.

The spread in the data points for the individual devices provided for each particular annealing time (Figure 5.5) stems from a number of nonidealities encountered in the experimental fabrication of the epitaxial GNR devices. First, although the average ribbon width was $W \sim 20$ nm, each individual GNR exhibited slight fluctuations in the

line width along the length of the entire ribbon, and similar fluctuations in line width were observed across the individual devices. The changes in the GNR width affected the capacitance of the device, which was used in the calculation of the Fermi energy. Therefore, slight changes in the Fermi energy from device to device were expected. In addition, previous research has suggested that atomic defects within the EG lattice manifest as local changes in the density of states [88], which translates into local changes in the carrier density. Because the data was obtained from individual devices fabricated on various regions of a larger EG sample, it was possible that some of the device regions tested showed local variations in the carrier density. Any existing carrier density fluctuation within a device would change the efficacy of the HSQ doping method; a larger intrinsic carrier density would require more oxygen to counteract the intrinsic doping and, therefore, such a device would exhibit a smaller Fermi energy shift as a function of doping. The opposite effect was expected for a smaller carrier density.

In summary, the first electrical transport measurements of chemically-doped, p-type epitaxial GNRs on SiC substrates have been shown. The use of the e-beam resist HSQ as a dopant source was found to be effective in counteracting the intrinsic, n-type doping of the EG on SiC (0001) [89]. The minimum conductivity point of the 20-nm, top-gate GNR transistors could be shifted by as much as +51 V through the simple thermal annealing of the HSQ. This shift corresponded to a change in the location of the Fermi level with respect to the Dirac point of ~ 0.45 eV. This work elucidates the detrimental effects to the p-type electrical transport properties of the EG as a result of HSQ doping, including a reduction in the mobility and a decrease in the on-off current ratio. These characterizations were lacking in the previous spectroscopic studies of EG

doping [79-82], and it is therefore difficult to determine what negative effects various alternate doping methods would have on the electrical transport of EG. The thermal annealing of HSQ represents a blanket method of doping an entire sample, but local methods to be implemented on the individual devices can be envisioned that use varying e-beam dosages [68] or current annealing to locally heat the HSQ. Such methods would locally add energy to the HSQ thin film and result in similar p-type doping effects. Furthermore, an alternate method to alleviate the strong, n-type doping of EG on SiC (0001) via hydrogen intercalation may provide for further chemical doping techniques to be implemented. Such a process will be described in the following section.

5.2 HYDROGEN INTERCALATION OF EPITAXIAL GRAPHENE

As discussed in Chapter 5.1, the intrinsic n-type doping of EG caused by the nonconducting buffer layer on SiC (0001) is problematic for complementary device formation. Although the HSQ doping technique was found to be capable of producing p-type epitaxial GNRs, the corresponding degradation of the electrical transport properties is undesirable for device functionality. An alternate doping method will be discussed in this section, whereby AG epitaxial samples (3.5 mm x 4.5 mm) were exposed to a high-temperature hydrogen anneal to alleviate the intrinsic n-type doping of the graphene. Although this technique represents a blanket method of doping large graphene regions as opposed to selective areas (i.e., nanoribbons), the ability to alleviate some of the heavy n-type doping of the EG may allow for innovative and selective doping techniques to be implemented in the future.

As briefly mentioned in Chapter II, EG produced on SiC (0001) is composed of a nonconducting interfacial layer, known as the buffer layer, and an EG monolayer. The buffer layer is structurally similar to monolayer graphene, but nearly 30% of the C atoms in this layer are covalently bound to the Si atoms in the bulk SiC substrate below [41]. The result of this covalent bonding is charge transfer between the substrate and the graphene monolayer, which serves as the source of the n-type doping intrinsic to EG on SiC (0001). This high level of doping limits the charge carrier mobility of the EG monolayer, and also makes device functionality problematic as the Dirac point is difficult to probe at large negative gate voltages [90].

The process of hydrogen intercalation has been used to successfully alleviate the n-type doping of EG on SiC (0001) and achieve what is known as quasi-free-standing monolayer graphene (QFS-MG) [79]. When EG is exposed to molecular hydrogen at high temperatures, but below the temperatures required for hydrogen etching or further graphitization of the samples, the nonconducting buffer layer is effectively converted into a graphene monolayer capable of electrical conduction (Figure 5.6 A). The result of this process is two-fold: the first graphene monolayer on top of the buffer layer is no longer heavily n-doped, and the charge carrier density of the first graphene monolayer, previously the buffer layer, is reduced. Simultaneously, the combined system of the buffer layer + the first EG monolayer becomes converted to a quasi-free-standing graphene bilayer (QFS-BG) (Figure 5.6 B). For the buffer layer + EG monolayer samples subjected to the hydrogen intercalation method, angle-resolved photoemission spectroscopy has previously revealed a shift of the Fermi energy slightly below the Dirac point, suggesting p-type doping of the EG [79]. These preliminary results suggest an

advantageous route to removing the n-type doping of the as-grown EG on SiC (0001) and achieving p-type epitaxial GNRs.

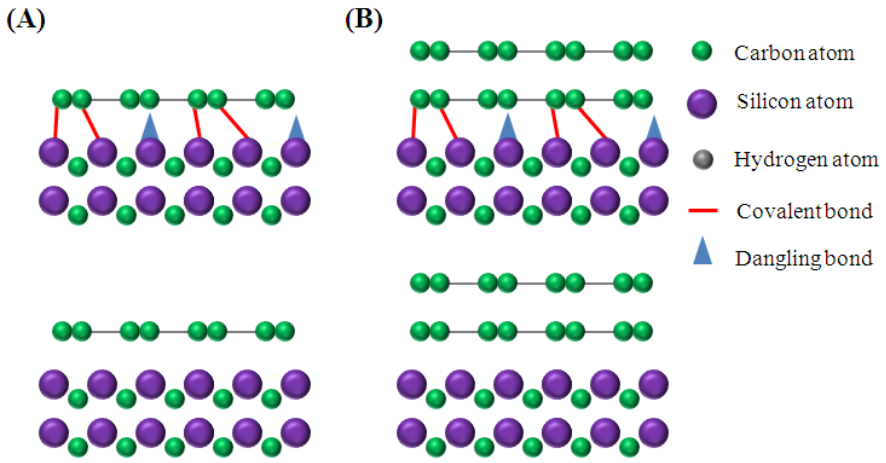

Figure 5.6. The process of hydrogen intercalation of EG on SiC (0001). (A) The buffer layer is first bound to the SiC substrate, and then converted to a QFS-MG upon exposure to hydrogen at high temperature. (B) The buffer layer + epitaxial graphene monolayer system is converted to QFS-BG.

Ultimately, to probe the doping effects of QFS-MG on SiC (0001), the graphene growth process would need to be tailored to produce only the buffer layer. Such a growth procedure is difficult to implement, as the growth time and temperature have to be highly regulated and optimized to prevent the premature growth of the first EG monolayer atop the buffer layer. In addition, the determination of the effective growth of only the buffer layer is challenging; advanced surface characterization techniques are required. The process of obtaining QFS-BG on SiC (0001) via hydrogen intercalation of the samples produced in this work was an achievable process, and worth investigation. Previous experimental work based on the transistor performance of bilayer graphene (obtained via the hydrogen intercalation of buffer layer + monolayer graphene) showed improved transistor performance [90], but the electrical measurements were performed on large area graphene

and therefore no insight into the graphene properties at the nanoscale was obtained. In general, the hydrogen intercalation process of EG on SiC (0001) is effective in shifting the majority charge carrier type from electrons to holes, and providing a corresponding increase in carrier mobility [90, 91]. In addition, understanding the electrical transport properties of epitaxial bilayer GNRs is an important goal, as limited data of this kind is currently available. With further process improvements in the production of EG on SiC (0001), a route to QFS-MG can be envisioned, thereby opening up avenues for further investigation into complementary doping techniques.

5.2.1 Process Development

Before the electrical measurements of the hydrogen-intercalated epitaxial GNRs (HI-GNRs) could be obtained, the intercalation process had to be developed and optimized. Starting with standard recipe variables from the literature [79, 90, 92], a similar process was developed for the CVD FirstNano graphene furnace (Table 11).

Table 11. Standard variables for the hydrogen intercalation of epitaxial graphene.

	Standard Variables from Literature	Experimental Variables
Temperature	600-1200 °C	1000-1100 °C
Pressure	600-760 Torr	600 Torr
Process Time	30-120 min.	30-120 min.

Before the hydrogen intercalation procedure was performed, the EG samples were hydrogen etched and graphitized with the processes described in Chapter II. In order to determine the efficacy of the hydrogen intercalation process, x-ray photoelectron spectroscopy (XPS) was performed on the EG samples both before and after the

intercalation process. Previous work has elucidated the spectra components related to the SiC substrate, the buffer layer, and the first EG monolayer in XPS and core-level photoelectron spectroscopy; a comparison to these results was used to confirm the efficacy of the developed hydrogen intercalation process [79, 90, 93]. The as-grown EG samples were found to exhibit the characteristic C *1s* peak for buffer layer + monolayer EG on SiC (0001) (Figure 5.7). The C *1s* peak is generally considered to be made up of four peaks: two representing the buffer layer, one representing the graphene monolayer, and one representing the SiC substrate.

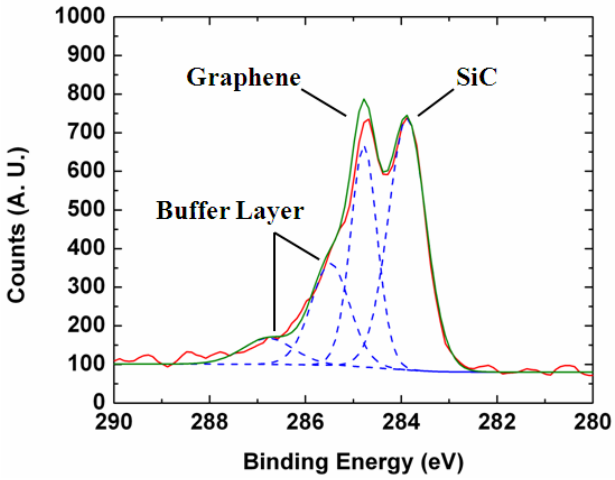

Figure 5.7. The XPS spectrum of the C *1s* peak of EG on SiC (0001). The raw data acquired (red), the envelope fit to the data (green), and the individual peaks (blue) are shown for clarity.

After the XPS analysis, the samples were transferred back to the CVD FirstNano graphene furnace for the hydrogen intercalation process. Numerous samples were exposed to the intercalation process with various temperatures and soak times, as well as H_2 flow rates. After the intercalation experiments, the XPS analysis of the samples was repeated to determine the optimized hydrogen intercalation process. At lower

temperatures and shorter soak times, the samples were found to be only partially intercalated with hydrogen, as evidenced by the presence of residual peaks related to the presence of the buffer layer (Figure 5.8 A). The samples subjected to the intercalation process at 1000 °C for 30 min. showed incomplete intercalation, as did the samples processed for soak times as long as 120 min. at the same temperature. In contrast, the samples processed at 1100 °C for 60 min. showed the full deconvolution of the graphene and SiC substrate peaks, suggesting complete hydrogen intercalation (Figure 5.8 B).

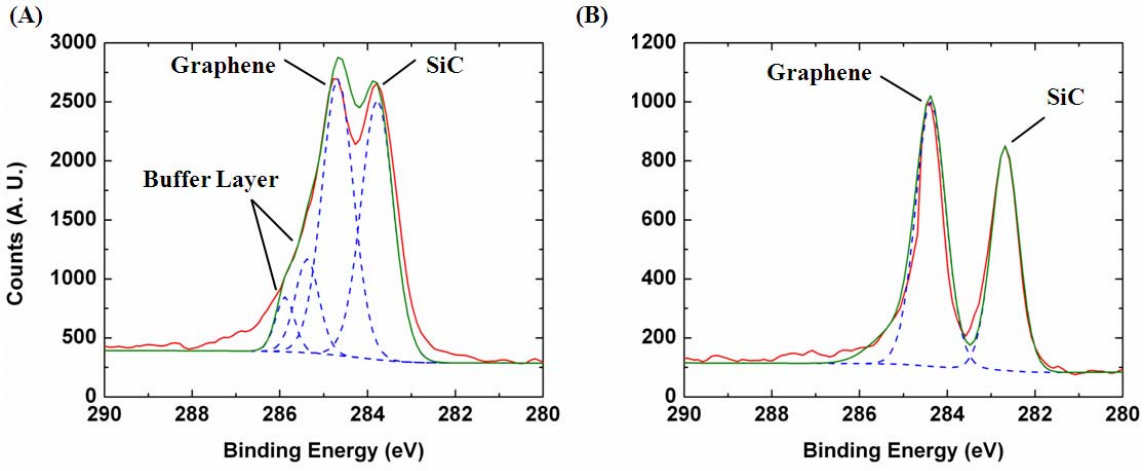

Figure 5.8. The XPS spectra of hydrogen-intercalated EG samples. The raw data acquired (red), the envelope fit to the data (green), and the individual peaks (blue) are shown for clarity. (A) Partially-hydrogenated EG. The residual peaks related to the buffer layer are visible. (B) Fully-hydrogenated EG. The peaks related to the buffer layer are no longer present, and the graphene and SiC peaks are fully separated.

Once the XPS spectra confirmed the development of a successful hydrogen intercalation process, AG and hydrogen-intercalated (HI) samples were subjected to van der Pauw electrical testing to determine changes in the EG sheet resistance. The AG samples exhibited a sheet resistance in the range of R_S = 800-1000 Ω/□, values that matched well with those reported in Chapter II. The HI samples displayed a lower sheet

resistance of R_S = 300-400 Ω/□; a similar reduction in the sheet resistance was found in the previous study of hydrogen-intercalated EG [90].

5.2.2 Electrical Properties of Hydrogen-Intercalated GNRs

The successful development of the hydrogen intercalation process for EG on SiC (0001) allowed for the subsequent fabrication of top-gated epitaxial GNR transistor devices. The process technology for the fabrication was identical to that presented in Chapter 3.1. GNRs of varying width (20 nm ≤ W ≤ 100 nm) were fabricated to estimate any changes in the size-dependent conductivity.

There were many expected implications of the hydrogen intercalation process on the electrical behavior of the epitaxial GNRs. First, the removal of the nonconducting buffer layer was expected to decrease the amount of intrinsic n-type doping of the EG, resulting in a positive shift of the minimum conductivity point. Most previous research of this kind has revealed p-type doping of the HI graphene, as opposed to the formation of truly charge-neutral EG. In addition to the expected p-type behavior of the HI graphene, the fabricated GNRs were expected to exhibit an even more exaggerated positive shift of V_{Gmin} due to the e-beam dosage used to expose the HSQ during the GNR patterning. As described in Chapter 5.1.1, the large e-beam dosages used to pattern the narrow GNRs used in this study (2100-4200 μC/cm^2) were expected to induce a positive shift of V_{Gmin} as a result of HSQ doping. Such a positive shift may not have been present in the experimental results presented in Chapter 5.1.2 due to the heavy, intrinsic n-type doping already present in the epitaxial GNRs on SiC (0001).

Second, the conversion of the monolayer system into an EG bilayer was expected to reduce the charge carrier density in the first graphene monolayer. The charge transfer mechanism between the first graphene monolayer (i.e., the previous buffer layer) and the substrate responsible for the intrinsic n-type doping of EG on SiC (0001) would no longer be applicable after the hydrogen intercalation. Due to the fact that the material system to be electrically tested after the hydrogen intercalation would be made up of both the first graphene monolayer, formerly the buffer layer, and the second graphene monolayer, formerly the EG monolayer, an increase in the charge carrier density was actually expected [90]. The electrical measurements would not be capable of probing the bottommost graphene monolayer only, as the contact electrodes were patterned on the upper graphene monolayer. The result expected in this work was an electrical characterization of QFS-BG. Although the charge carrier density was expected to increase after the hydrogen intercalation process, the mobility was similarly expected to increase and manifest as improvements in the electrical transport properties.

Finally, the use of a graphene bilayer in the transistor device, as opposed to a monolayer atop the nonconducting buffer layer, was expected to induce significant changes in the switching efficacy. Due to screening effects and the inability to definitively contact more than one graphene monolayer with the electrodes, the lower graphene monolayer may not be sufficiently controlled by the top gate. The result was expected to be a reduced on-off current ratio of the bilayer transistor device.

For the electrical characterization of the hydrogen intercalation process, a batch of samples were selected for comparison based on similarities in AG sheet resistance, charge carrier density, and morphology as characterized by AFM imaging. Electrical

measurements were performed at T = 77 K with a Keithley 2612 source meter in the four-point mode, as outlined in Chapter 5.1.2. The electrical transport measurements of two representative devices, one tested with AG-GNRs (pre-intercalation) and one tested with HI-GNRs (post-intercalation), are shown in Figure 5.9. The AG-GNRs showed a negative minimum conductivity point of V_{Gmin} = -75 V, corresponding to an n-type carrier density of ~ 1.6 x 10^{13} cm^{-2}. In contrast, the HI-GNRs showed a minimum conductivity point of V_{Gmin} = +88 V, corresponding to a larger p-type carrier density of ~ 1.9 x 10^{13} cm^{-2}.

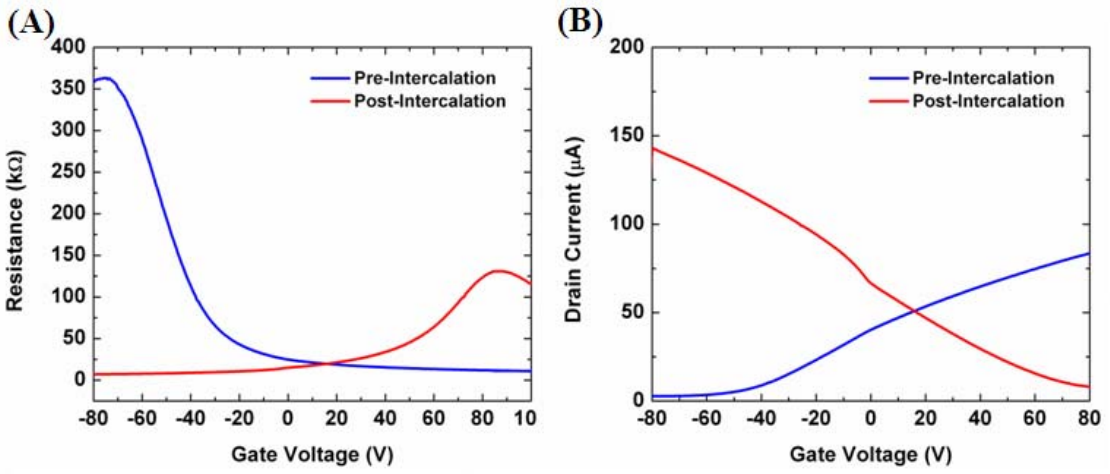

Figure 5.9. The electrical transport measurements of 20-nm GNR transistor devices. The red curves pertain to AG-GNRs, and the blue curves pertain to HI-GNRs. (A) The resistance vs. gate voltage and (B) the current vs. gate voltage is plotted. Upon hydrogen intercalation, the electrical data reveals a strong positive shift of V_{Gmin}, a reduced I_{on}/I_{off}, and a slightly reduced resistance far from the charge-neutrality point for the hydrogen-intercalated sample.

In order to estimate any improvements in the GNR mobility, the mobility was calculated according to the procedure outlined in Chapter 5.1.2 with a set reference carrier density of n = 7.2 x 10^{12} cm^{-2}. To estimate any changes in the mobility as a result of the p-type doping upon hydrogen-intercalation, the mobility of a 20-nm epitaxial GNR was calculated for both the AG samples and the HI samples. For the AG-GNRs, the

average mobility was found to be μ = 820 cm^2/V-s, and for the HI-GNRs, the average mobility increased by ~ 50% to μ = 1260 cm^2/V-s. In addition, although the modulation of the HI-GNRs was significantly reduced as compared to the AG-GNRs (I_{on}/I_{off} ~ 33), the value remained relatively large (I_{on}/I_{off} ~ 19*)* as compared to similar electrical measurements of ExG devices. The off-state resistance was also found to be similar before and after the hydrogen intercalation, suggesting that the top gate was able to control conduction in the bottom graphene monolayer and effectively switch the device.

To further elucidate the p-type doping achieved with the hydrogen intercalation process, the Fermi level was determined according to the procedure outlined in Chapter 5.1.2. The charge carrier density was evaluated at the minimum conductivity point, and then used to estimate the shift of the Fermi level as a result of the hydrogen intercalation. For the non-intercalated sample, E_F = 0.41 eV, which agrees well with the theoretical estimation that intrinsic EG on SiC (0001) should display a Fermi energy ~ 0.4 eV above the Dirac point. After the hydrogen intercalation, the Fermi energy shifted by ~ -0.8 eV to E_F = -0.45 eV, revealing that the Fermi energy now appeared in the lower portion of the Dirac cone as expected for p-type graphene.

Although p-type EG was achieved with the hydrogen intercalation method, it was important to compare the electrical transport results to the work presented in Chapter 5.1, whereby an alternate doping technique was used to obtain p-type EG. The previous work based on HSQ doping showed a significant degradation of the electrical transport properties as a result of charged impurity scattering. In contrast, the hydrogen intercalation method was not expected to induce similar degradation due to the lack of charged impurities provided during the process. A comparison of the HI-GNR sample

and the thermally-annealed HSQ sample from the study in Chapter 5.1.2 is shown in Figure 5.10. The original gate voltage sweep performed on the thermally-annealed HSQ sample had to be kept below +40 V to avoid premature breakdown of the gate; a full comparison of the entire sweep (-60 V to +100 V) used on the HI-GNR sample was not possible for that reason. The thermally-annealed HSQ sample displays V_{Dirac} significantly closer to a gate voltage of 0 V, but the electrical properties of the device are poor in comparison to the HI-GNR sample. Specifically, by considering the mobility of the 20-nm GNRs at the same carrier density (n = 7 x 10^{12} cm^{-2}), the HI-GNR sample displays a mobility of μ = 1260 cm^2/V-s, while the thermally-annealed HSQ sample only achieves a maximum mobility of μ = 30 cm^2/V-s. The modulation of the HI-GNR sample (I_{on}/I_{off} = 19) was significantly better than that of the thermally-annealed sample (I_{on}/I_{off} = 5). In addition, the lower resistance values of the HI-GNR sample allow for an improved drain current and an increased current-carrying capacity above that afforded by the thermally-annealed HSQ sample. These results suggest that hydrogen intercalation, rather than thermal annealing of HSQ, represents a more advantageous route to achieving p-type EG.

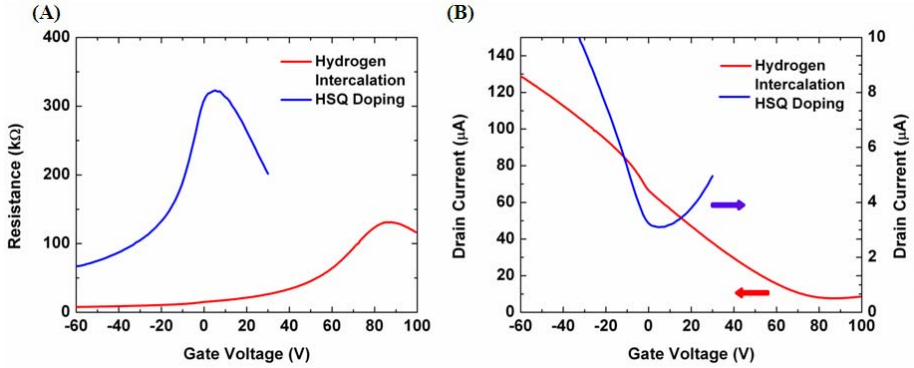

Figure 5.10. A comparison of the electrical transport behavior of p-type epitaxial GNRs produced by the hydrogen intercalation and the HSQ doping methods. The GNR width was 20 nm. (A) The resistance vs. gate voltage and (B) current vs. gate voltage are plotted for the hydrogen intercalation sample (red) and the thermally-annealed HSQ doping sample (blue).

Further analysis and comparison to the size effect data provided in Chapter 3.3 was performed to estimate any changes in the size-dependent conductivity as a result of the hydrogen intercalation process. The increased charge carrier density was expected to further enhance the LER scattering [94], but the change from n-type to p-type charge carriers as a result of the hydrogen intercalation was also expected to improve the mobility. To determine the 2D resistivity of the GNR devices studied in this work, the device resistance was measured at a gate voltage of 0 V. The devices were electrically tested in the four-point mode before and after the top-gate oxide application to determine any changes in the device resistance that may have skewed an accurate comparison to the samples presented in Chapter 3.3. A negligible change ($< \pm 5\%$) in the resistance of the GNR devices after the device fabrication was seen for all the samples tested.

In Figure 5.11, the hydrogen intercalation size effect is shown alongside the results from a high-quality and low-quality EG sample used in the original size-dependent conductivity study. Two representative HI-GNR devices are shown to exhibit resistivity values at all GNR line widths similar to that found previously for high-quality, EG monolayer samples (Sample R4), and similarly, to exfoliated GNRs. More than ten devices of this kind (i.e., HI-GNRs) were tested, and the resulting data was found in a tight range between the two curves shown in green in Figure 5.11. When considering the model fit to the data, as derived in Chapter 3.3, the HI-GNR samples were seen to achieve significantly larger mobilities, smaller 2D resistivities, and a decreased threshold line width in comparison to the low-quality EG (Sample G6) initially tested (Table 12).

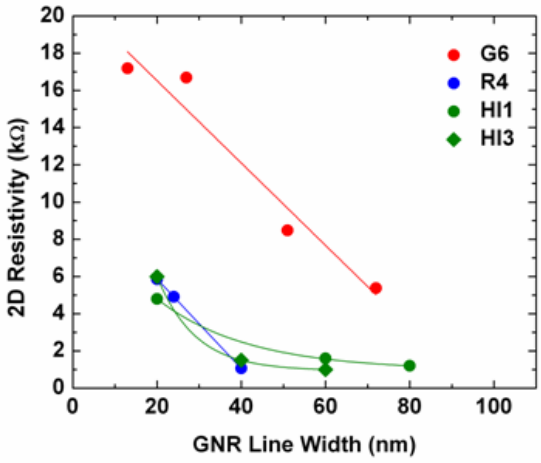

Figure 5.11. The 2D resistivity vs. GNR line width of the hydrogen intercalation samples. The red and blue curves pertain to the best (blue) and worst (red) size effect data collected in the initial size-dependent conductivity study, and are meant as a reference to the new data.

Table 12. The mobility and model parameters of a 50-nm GNR on both AG epitaxial samples and the hydrogen-intercalated samples.

Sample	Terrace Angle (°)	W_{th} (nm)	B	μ_{2D} (Hall)	μ_W (50 nm)	μ_{GNR} (50 nm)	ρ_{GNR} (50 nm)
R4	0	32	3.75	4740	25008	3985	1120
G6	90	942	0.74	2639	218	201	7775
HI1	45	29	3.5	5010	35355	4388	1138
HI3	45	31	3.8	5520	35727	4781	1044

The model parameters for the HI-GNR samples suggest behavior similar to that found for exfoliated GNRs on SiO_2/Si substrates [67]. The value of the exponent *B* for Samples HI1 and HI3 was similar to that found for high-quality EG samples on SiC (0001). The HI-GNR samples display similar threshold line widths as well, suggesting that boundary scattering did not play a prominent role in the mobility degradation as a function of the line-width scaling. In contrast, the similarity to the exfoliated GNR behavior suggests that the size-dependent conductivity for HI-GNRs was influenced more heavily by the LER. This was expected, as the increased carrier density of the HI-GNRs

was predicted to increase the LER scattering [94]. Upon comparing the HI-GNR samples to the size effect work in Chapter 3.3, the resistivities at all line widths were significantly less than both moderate- and low-quality non-intercalated samples. The average mobility for a 50-nm GNR fabricated with non-intercalated EG was found to be $\mu \sim 2000$ cm^2/V-s, while the average mobility for a 50-nm GNR fabricated with hydrogen-intercalated EG was found to be $\mu \sim 4500$ cm^2/V-s, an improvement of more than 125%. These results suggest that the creation of QFS-BG reduces the influence of the boundary scattering from the SiC substrate. In turn, the charge carrier mobility remains high even at extremely narrow GNR line widths.

Due to the similarity between the electrical results of the HI-GNR samples and the best AG-GNR sample from the original size-dependent conductivity study, the substrate morphology of the samples was carefully compared. This analysis was performed to estimate whether the substrate morphology of the HI-GNR samples was somehow improved over the previous samples, or whether the hydrogen intercalation process alone was capable of achieving an improved size effect. The AFM images of the three samples are shown in Figure 5.12. The terrace angle with respect to the substrate edge for Samples HI1 and HI3 was found to be identical (~ 45°), and the terrace structure was significantly more nonuniform in comparison to Sample R4. The images reveal that the substrate morphology was not improved at some point between the original size-dependent conducitivity study and the hydrogen intercalation work. In contrast, the morphology appears more similar to the low- and moderate-quality samples presented in Chapter 3.3, yet the electrical properties of the HI-GNR samples was much improved

over the original AG-GNR samples. Therefore, the hydrogen intercalation process appears to improve the size-dependent conductivity of identically-sized GNRs.

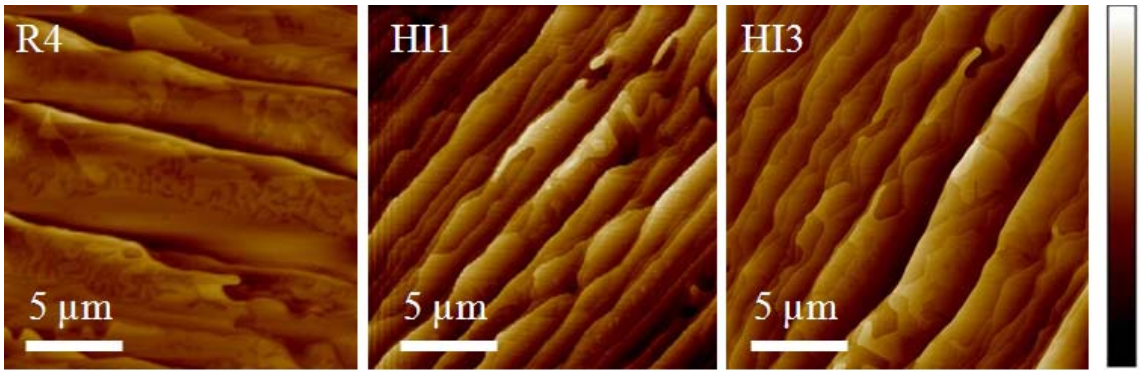

Figure 5.12. AFM images (20 x 20 µm^2) of the high-quality AG sample (R4) and the two HI samples (HI1 and HI3) used in the size-dependent conductivity study. The gradient scale bar corresponds to a 10-nm height variation. The morphology of Samples HI1 and HI3 are similar, but do not exhibit the smooth, large, straight edge terraces observed on the high-quality, AG sample (R4).

The two chemical doping techniques presented in this chapter, the thermal annealing of HSQ and the intercalation of EG with hydrogen, were both found to be capable of achieving p-type EG. The HSQ doping method was found to be capable of shifting the Fermi energy of the EG monolayer below the Dirac point by functionalizing the graphene surface with oxygen. Unfortunately, the O atoms appear to act as charged impurities, thereby increasing the carrier scattering and degrading the electrical transport properties. In contrast, the optimized hydrogen intercalation process was also found to be capable of producing p-type EG without the same detrimental effects to the electrical transport. When considering the efficacy of using QFS-BG as opposed to the buffer layer + monolayer system, the electrical data suggests improved behavior over that afforded by AG-GNR samples on SiC (0001). In addition, the size-dependent conductivity of HI-GNR samples was found to agree quite closely with the best results presented in Chapter

3.3. The size effect appeared to match up with high-quality, AG samples, and similarly, to exfoliated GNRs on SiO_2/Si substrates. A careful study of the HI-GNR samples used in the size-dependent conductivity study revealed a rough substrate morphology that would be characterized as low- to moderate-quality AG samples such as those studied in Chapter 3.3. Even with a less than desirable substrate or a careful alignment of the GNRs along the SiC terraces, the mobility values of the HI-GNR samples were significantly improved over that of AG-GNR or thermally-annealed HSQ samples. The results presented in this chapter suggest that the hydrogen intercalation of monolayer EG on SiC (0001) can be used to achieve high-quality, p-type bilayer EG which can be effectively used in graphene-based transistors.

CHAPTER VI – CONCLUSIONS

The major goal of this work was to provide a systematic investigation of the novel structural and electrical properties of epitaxial graphene at the nanoscale. The importance of graphene continues to steadily increase as the semiconductor industry looks to alternate material systems to replace or become integrated with silicon in the next decade and beyond. The scaling issues related to current silicon technology can be circumvented by utilizing graphene as the channel material in FET devices and as both local and global interconnects. With graphene as a component in the next generation of integrated circuitry, nanoscale devices with improved performance over that currently afforded by silicon can be realized.

The first part of this work was based on the optimization of epitaxial graphene growth on SiC substrates. By using a custom-designed vacuum furnace, high-quality epitaxial graphene was produced; the quality of the graphene was fully characterized with both structural and electrical techniques. Although the epitaxial graphene produced in this work exhibited morphological and electrical characteristics on par with other material presented in the literature, further advances in the surface preparation of the SiC substrate and the quality of the graphitization may open up new avenues for achieving even better quality material for integration with silicon technology. Ultimately, the goal of epitaxial graphene growth, important for future use by the semiconductor industry, should be large-area, terrace-free substrates, improved graphene grain boundary sizes, and monolayer graphene growth on the wafer-scale.

The second part of this work was based on a careful study of the conductivity of epitaxial graphene nanoribbons as the feature sizes were scaled below one μm. The importance of graphene nanoribbons was highlighted in the introduction, where it was explained that an effective band gap can be induced in the material by laterally confining the charge carriers via the creation of nanoribbons. In order for graphene to function at a level comparable to current silicon MOSFETs, the switching efficacy of graphene-based transistors must be improved by utilizing the band gap induction technique. In the study, the size-dependent conductivity was found to be a function of both the lithographically-patterned line-edge roughness of the nanoribbons and the morphology of the SiC substrates. Both the line-edge roughness and the substrate morphology can be further improved to keep the conductivity of nanoscale epitaxial graphene at a high level, thereby providing a route for further research into the efficacy of band gap induction. The mitigation of the line-edge roughness can be achieved through a number of novel functionalization and production techniques which draw knowledge from the realms of chemistry, materials science, and process development. The alteration of the SiC substrate morphology is heavily based on materials science, as the growth and surface preparation parameters must be finely tuned and carefully controlled to provide an optimum starting substrate for epitaxial graphene production. The size-dependent conductivity study served to elucidate the sources of the detrimental effects to the mobility of epitaxial graphene at the nanoscale.

The third part of this work was based on the mitigation of the line-edge roughness to further improve the size-dependent conductivity. The functionalization of selective regions of epitaxial graphene nanoribbons with hydrogen was presented as a method to

alleviate line-edge roughness scattering, and keep the graphene nanoribbon mobility large at narrow line widths. By utilizing a novel technique, whereby only the extreme edges of graphene nanoribbons were exposed to the hydrogen functionalization, the line-edge roughness was effectively removed, allowing for improved conductivity at the nanoscale. The results presented in this study showed a significant improvement in the size-dependent conductivity as compared to the previous work based on non-functionalized epitaxial graphene nanoribbons. The functionalization of graphene with any number of interesting atomic species can be used to provide a high level of control over graphene's unique electrical properties. Current and future work based on a broad study of different atomic species and functionalization techniques opens up new avenues into exploiting the intrinsic, highly beneficial, electrical properties of graphene at the nanoscale.

The last part of this work was based on an investigation of two distinct techniques that allow for the tunable and controllable doping of epitaxial graphene. As described in this work, epitaxial graphene produced on SiC (0001) suffers from intrinsic, heavy, n-type doping which limits the ability of graphene to be used in any complementary manner. The application of hydrogen to the basal plane of epitaxial graphene was shown to counteract this n-type doping, and allow for the first realization of p-type epitaxial graphene nanoribbons. The doping method described, based on the thermal annealing of the negative-tone e-beam resist HSQ, was found to be detrimental to the electrical transport properties of the nanoribbons. In order to utilize p-type epitaxial graphene without experiencing any significant degradation of the mobility or the switching efficacy of transistor devices, an alternate doping technique was realized based on the intercalation of hydrogen underneath epitaxial graphene films on the SiC substrates. The

results of this technique were found to be highly advantageous; p-type epitaxial graphene was achieved that exhibited an improved size-dependent conductivity over that afforded by intrinsic, n-type material. Future work based on a combination of the two presented doping techniques suggest a route towards the effective control of epitaxial graphene doping levels in order to fabricate complementary devices and accurately design graphene-silicon integrated devices.

In addition to the specific studies of epitaxial graphene nanoribbons presented herein, a significant amount of process technology was developed. Not only was the production of high-quality epitaxial graphene achieved, but the careful characterization procedures (AFM, Raman spectroscopy, XPS, van der Pauw and Hall effect testing) necessary to understand the produced material were fully optimized and implemented. The creation of a top-gate, graphene-based transistor was realized through a series of lithography (photolithography and e-beam), plasma etching, thin film deposition (metal and oxide), and thermal annealing for surface cleaning; all the process parameters were finely tuned and optimized to provide a robust graphene device for electrical characterization of the material. Furthermore, the development of functionalization techniques, including the careful control of HSQ etching, hydrogen attachment via plasma exposure, thermal annealing of HSQ, and hydrogen intercalation of the epitaxial graphene, were also all developed and implemented. The end results of the myriad development and optimization techniques for each particular process was the key to allowing for the investigation of epitaxial graphene behavior at the nanoscale.

In conclusion, the major goals highlighted in the introduction of this work were achieved. A careful study of the structural and electrical properties of epitaxial graphene

at the nanoscale highlighted the detrimental effects to the graphene mobility. Novel techniques meant to counteract or alleviate the mobility degradation as a function of scaling were proposed, and successfully implemented. Epitaxial graphene nanoribbons were shown to perform equal to or better than exfoliated graphene, the current material of choice for most graphene-based research, but a less than desirable candidate for the large-scale production required by the semiconductor industry. The results presented in this work suggest that epitaxial graphene is truly a strong contender to replace or become integrated with silicon technology in the near future.

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